73002BZ

user's guide

TECHNICAL WRITING SERVICES

Integrated Circuits

FOXBORO

FOXBORO

user's guide

Integrated Circuits

73002BZ-A

FOXBORO INTEGRATED CIRCUITS

S.K. 19227

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Foxboro, Massachusetts 02035

HISTORY

Version	Date	Copies	Remarks
A	10/73	200	Original edition

PREFACE

This book (document 73002BZ) is intended as an aid to maintenance personnel servicing process management and control equipment such as FOX 2 Systems. It contains information necessary to trace signals through or replace integrated circuits (ICs). ICs described herein are used in standard system components manufactured by The Foxboro Company. ICs in standard system components, such as computers, drums, CRT consoles, etc. that are part of the Foxboro product line, but not manufactured by The Foxboro Company, are not included.

Foxboro part numbers and equivalent IC manufacturer's part numbers are identified in Table 1. This table can be used as a parts substitution list in the replacement of integrated circuits.

All integrated circuits described in this standard book might not be in any given system, and any ICs for custom modules designed specifically for your system are not covered in this standard book.

IC information is presented in Foxboro part number sequence, as indicated in the table of contents. Pages are not numbered, so information on an IC is located relative to the alpha-numeric part number sequence.

Table 1. Integrated Circuit Cross Reference Data

FOXBORO	T.I.	N.S.C	SPRAGUE	MOTOROLA	FAIRCHILD	DEC	SIGNETICS
C3002RR	SN75110N						
C3004NS	SN75107N						
C3004NT	SN7403N	DM8003N	USN7403				
C3004NW	SN7404N	DM8004N	USN7404	MC7404P			
C3004PL	SN74121						
C3007MR	SN7405N		USN7405A	MC7405P			
C3008BZ	SN74107						
C3008FL	SN7442						
C3009SM					9093		
C3009SS					9959		
C3009ST							N8T01B
C3313AA						380A	
C3313AB						8881	
C3313AC	SN7407						
C3313AD	SN74H78-N-						
C3313AE	SN7486-N						

Table 1. Integrated Circuit Cross Reference Data (continued)

FOXBORO	T.I.	NSC	SPRAGUE	MOTOROLA	FAIRCHILD	DEC	SIGNETICS
C3313AF	SN74164						
C3313AG	SN7406-N						
C3313AH	SN7417						
C3313AJ	SN7437						
C3313AL							SP384A
C3313AP	SN7440J		USN7440AJ	MC7440L			N7440F
C3313AQ	SN7474J		USN7474J				
C3313AR	SN7405J		US7405J	MC7405L			
C3313AS	SN74121J						N74121F
C3313AT			US7439H				
V3008EA	SN7400N	DM8000N	USN7400A	MC7400P			
V3008EB	SN7401N		USN7401A	MC7401P			
V3008EC	SN7402N		USN7402A	MC7402P			
V3008EE	SN7410N	DM8010N	USN7410A	MC7410P			
V3008EF	SN7420N	DM8020N	USN7420A				
V3008EK	SN7430N		USN7430A	MC7430P			
V3008EL	SN7440N	DM8040N	USN7440A	MC7440P			

Table 1. Integrated Circuit Cross-Reference Data (continued)

FOXBORO	T.I.	N.S.C	SPRAGUE	MOTOROLA	FAIRCHILD	DEC	SIGNETICS
V3008EN	SN7450N		USN7450A	MC7450P			
V3008EP	SN7451N		USN7451A	MC7451P			
V3008ER	SN7453N		US7453A	MC7453P			
V3008ES	SN7454N		US7454A	MC7454P			
V3008ET	SN7460N		USN7460A	MC7460P			
V3008EW	SN7470N		US7470A				
V3008EX	SN7472N		SUN7472A	MC7472P			
V3008EY	SN7473N	DM8501N	USN7473A	MC7473P			
V3008EZ	SN7474N	DM8510N	USN7474A				
V3008FA	SN7475N	DM8550N	USN7475B	MC7475P			
V3008FB	SN7476N	DM8500N	USN7476B	MC7476P			
V3008FC	SN7480N		USN7480A				
V3008FE	SN7482N		USN7482A				
V3008FF	SN7483N		USN7483B				
V3008FK	SN7490N	DM8530N	USN7490A				
V3008FL	SN7491AN		USN7491A				

Table 1. Integrated Circuit Cross-Reference Data (continued)

FOXBORO	T.I.	N.S.C	SPRAGUE	MOTOROLA	FAIRCHILD	DEC	SIGNETICS
V3008FM	SN7492N	DM8532N	USN7492N				
V3008FN	SN7493N	DM8533N	USN7493A				
V3008FP	SN7494N						
V3008FR	SN7495N						
V3008FS	SN7496N						

KEY:

FOXBORO = The Foxboro Company, Foxboro, Ma.
T. I. = Texas Instruments Inc., Dallas, Texas
N.S.C = National Semiconductor Corp., Santa Clara, Ca.
SPRAGUE = Sprague Electric Co., North Adams, Ma
MOTORLA = Motorola Semiconductor Products Inc., Phoenix, Ar
FAIRCHILD = Fairchild Camera & Instrument Corp., Mountain View, Ca
DEC = Digital Equipment Corp., Maynard, Ma
SIGNETICS = Signetics Corp., Sunnyvale, Ca

CONTENTS

CONTENTS (continued)

FIRST USED ON	REVISIONS				
C3001XX	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN 3035.	A.Z.	16DEC69	JEH

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Dual Line Driver

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 3,4,5

4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN75110N

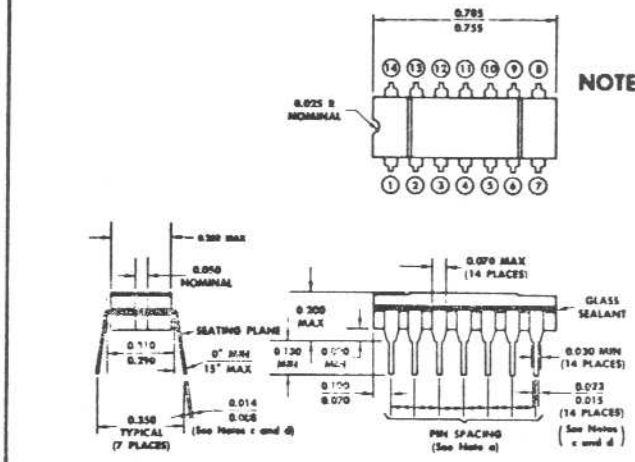
NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

NOTES:

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED REMOVE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES ALL DIMS APPLY AFTER PLATING TOLERANCES ON FRACTIONS: ± 1/64 DECIMALS: ± .005 ANGLES: ± 1/2° MATERIAL: FINISH:	WORK AUTH NO.		FOXBORO THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
	DRAFTSMAN AZIKAS	DATE	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN75110N
	DESIGNER		
	CHECKER JE Hatch	16DEC69	
	ENGINEER		SIZE A | SYMBOL B | DRAWING NO. C3002RR | REV A
	RELEASED		
	LOCAL RELEASE		SCALE: NONE | SHEET 1 OF 5

FORM 5083A (6/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

SIZE	SYMBOL	DRAWING NO.	REV
A	B	IC3002RR	A
	SCALE:		SHEET 2 OF

NOT SCALE PRINT

A 5083B (6/67)

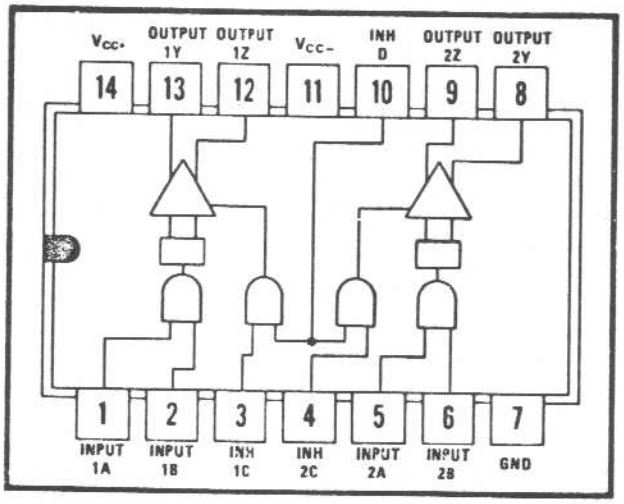
logic

TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the on state

High output represents the off state



SIZE	SYMBOL	DRAWING NO.	REV
A		C3002RR	A
SCALE:		SHEET 3 OF	

NOT SCALE PRINT

5085B (6/67)

absolute maximum ratings (over operating free-air temperature range unless otherwise noted)

Supply voltage V_{CC+} (See Note 1) . . . . . 7 V
Supply voltage V_{CC-} (See Note 1) . . . . . –7 V
Logic and inhibitor input voltages (See Note 1) . . . . . 5.5 V
Common-mode output voltage (See Note 1) . . . . . –5 to 12 V
Operating free-air temperature range, Series 55 . . . . . –55°C to 125°C
Series 75 . . . . . 0°C to 70°C
Storage temperature range, ceramic dual-in-line (J) package . . . . . –65°C to 150°C
plastic dual-in-line (N) package . . . . . –55°C to 150°C

recommended operating conditions (see note 2)

	SN55109, SN55110			SN75109, SN75110			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC+} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-} (See Note 1)	–4.5	–5	–5.5	–4.75	–5	–5.25	V
Positive common-mode output voltage (See Note 1)	0		10	0		10	V
Negative common-mode output voltage (See Note 1)	0		–3	0		–3	V
Operating free-air temperature range	–55		125	0		70	°C

NOTES: 1. These voltage values are with respect to the network ground terminal.
2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

SIZE A | SYMBOL S | DRAWING NO. C3002RR | REV A
DO NOT SCALE PRINT | SCALE: | SHEET 4 OF 5
FORM 5083B (6/67)

electrical characteristics (over operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN55109, SN75109			SN55110, SN75110			UNIT
					MIN	TYP§	MAX	MIN	TYP§	MAX	
$I_{IH(L)}$	High-level input current into 1A, 1B, 2A or 2B	16	V_{CC+} = MAX, $V_{IH(L)}$ = 2.4 V	V_{CC-} = MAX,			40			40	μA
			V_{CC+} = MAX, $V_{IH(L)}$ = MAX V_{CC+}	V_{CC-} = MAX,			1			1	mA
$I_{IL(L)}$	Low-level input current into 1A, 1B, 2A or 2B	16	V_{CC+} = MAX, $V_{IL(L)}$ = 0.4 V	V_{CC-} = MAX,			−3			−3	mA
$I_{IH(I)}$	High-level input current into 1C or 2C	17	V_{CC+} = MAX, $V_{IH(I)}$ = 2.4 V	V_{CC-} = MAX,			40			40	μA
			V_{CC+} = MAX, $V_{IH(I)}$ = MAX V_{CC+}	V_{CC-} = MAX,			1			1	mA
$I_{IL(I)}$	Low-level input current into 1C or 2C	17	V_{CC+} = MAX, $V_{IL(I)}$ = 0.4 V	V_{CC-} = MAX,			−3			−3	mA
$I_{IH(I)}$	High-level input current into D	17	V_{CC+} = MAX, $V_{IH(I)}$ = 2.4 V	V_{CC-} = MAX,			80			80	μA
			V_{CC+} = MAX, $V_{IH(I)}$ = MAX V_{CC+}	V_{CC-} = MAX,			2			2	mA
$I_{IL(I)}$	Low-level input current into D	17	V_{CC+} = MAX, $V_{IL(I)}$ = 0.4 V	V_{CC-} = MAX,			−6			−6	mA
$I_{O(on)}$	On-state output current	18	V_{CC+} = MAX,	V_{CC-} = MAX			7			15	mA
			V_{CC+} = MIN,	V_{CC-} = MAX	3.5			6.5			mA
$I_{O(off)}$	Off-state output current	18	V_{CC+} = MIN,	V_{CC-} = MIN			100			100	μA
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled	19	$V_{IL(L)}$ = 0.4 V,	$V_{IH(I)}$ = 2 V		18	30		23	35	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled	19	$V_{IL(L)}$ = 0.4 V,	$V_{IH(I)}$ = 2 V		−18	−30		−34	−50	mA
$I_{CC+(off)}$	Supply current from V_{CC+} with driver inhibited	19	$V_{IL(L)}$ = 0.4 V,	$V_{IL(I)}$ = 0.4 V		18			21		mA
$I_{CC-(off)}$	Supply current from V_{CC-} with driver inhibited	19	$V_{IL(L)}$ = 0.4 V,	$V_{IL(I)}$ = 0.4 V		−10			−17		mA

‡For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions for the applicable device type.

§All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH(L)}$	Propagation delay time, low-to-high level, from logic input A or B to output Y or Z	20	R_L = 50 Ω,	C_L = 40 pF		9	15	ns
$t_{PHL(L)}$	Propagation delay time, high-to-low level, from logic input A or B to output Y or Z	20	R_L = 50 Ω,	C_L = 40 pF		9	15	ns
$t_{PLH(I)}$	Propagation delay time, low-to-high level, from inhibitor input C or D to output Y or Z	20	R_L = 50 Ω,	C_L = 40 pF		16	25	ns
$t_{PHL(I)}$	Propagation delay time, high-to-low level, from inhibitor input C or D to output Y or Z	20	R_L = 50 Ω,	C_L = 40 pF		13	25	ns

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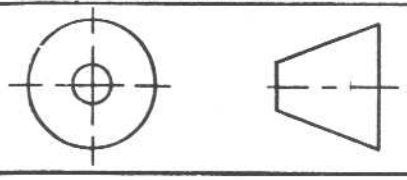
THIRD ANGLE PROJECTION



REVISIONS

SYM	CHANGE NO.	DATE	APP
A	LOCAL RELEASE ECN 3035	16 DEC 69	EH

NS C3001XX

FIRST USED ON

GR

APPLICATION

DO NOT SCALE DRAWING

1. DESCRIPTION

Circuit, Integrated (dual in-line package) hex inverter

2. PHYSICAL CHARACTERISTICS

See Sheet 2

3. PERFORMANCE CHARACTERISTICS

See Sheet 3 & 4

4. MANUFACTURER'S NAME & PART NO.

Texas Instruments, Part No. SN75107N

PRINT DISTR DEPT	QTY

FOR PARTS LIST SEE DWG PL

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

.X ± | .XX ±.04 | .XXX ±.010

ANGLES ± FRACTIONS ± | ⊕ .028 DIA

MATL

FINISH

DRAWN	EH	DATE
CHECKED	EH	16DEC69
DESIGNED		
DRAFTING		
RESTRICTED RELEASE		
LOCAL RELEASE	EH	16DEC69
CORPORATE RELEASE		

FOXBORO

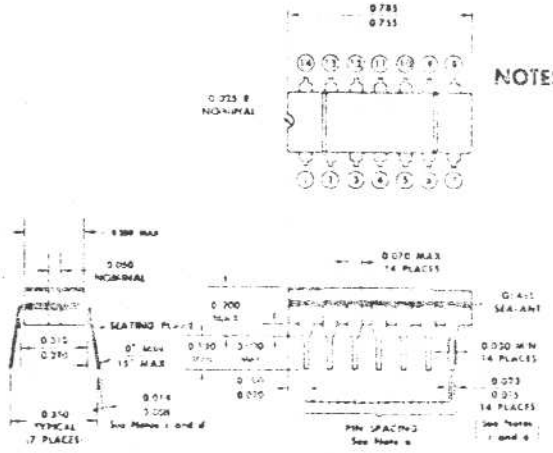
THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE

Circuit, Integrated
Dual In-line Package
Type SN75107N

SIZE	DWG CODE	DRAWING NUMBER	REV
A		C3004NS	A

SCALE | WT | SHEET 1 OF 4



NOTES:
a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11).
b. All dimensions in inches unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.
e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

SIZE	SYMBOL	DRAWING NO.	REV
A		C3004NS	A
		SCALE:	SHEET 2 OF

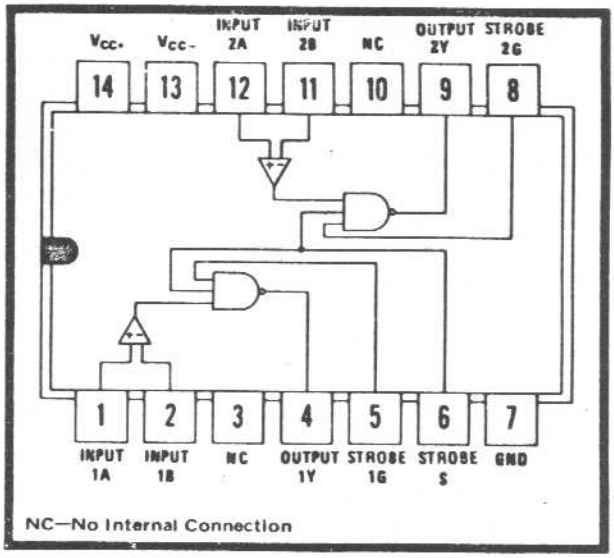
DO NOT SCALE PRINT

FORM 30838 (6/67)

logic

TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} < 25$ mV	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L



NC—No Internal Connection

SIZE	SYMBOL	DRAWING NO.	REV
A	D	TC3004NS	A
	SCALE:		SHEET 3 OF 4

DO NOT SCALE PRINT

5083B (6/67)

absolute maximum ratings (over operating free-air temperature range unless otherwise noted)

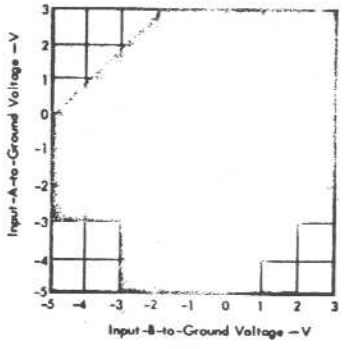
Supply voltage V_{CC+} (See Note 1) . . . . . 7 V
Supply voltage V_{CC-} (See Note 1) . . . . . −7 V
Differential input voltage (See Note 2) . . . . . ±6 V
Common-mode input voltage (See Note 1) . . . . . ±5 V
Strobe input voltage (See Note 1) . . . . . 5.5 V
Operating free-air temperature range, Series 55 . . . . . −55°C to 125°C
Series 75 . . . . . 0°C to 70°C
Storage temperature range, ceramic dual-in-line (J) package . . . . . −65°C to 150°C
plastic dual-in-line (N) package . . . . . −55°C to 150°C

recommended operating conditions (see note 3)

	SN55107, SN55108			SN75107, SN75108			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC+} (See Note 1)	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-} (See Note 1)	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Output sink current			−16			−16	mA
Differential input voltage (See Notes 2 and 4)	−5†		5	−5†		5	V
Common-mode input voltage (See Notes 1 and 4)	−3†		3	−3†		3	V
Input voltage range, any differential input to ground (See Note 4)	−5†		3	−5†		3	V
Operating free-air temperature range	−55		125	0		70	°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. These voltage values are at the noninverting (+) terminal with respect to the inverting (−) terminal.
3. When using only one channel of the line receiver, the inputs of the other channel should be grounded.
4. The recommended combinations of input voltages fall within the shaded area of the figure at the right.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES FOR LINE RECEIVERS



† The algebraic convention, where the most positive limit is designated maximum, is used in this data sheet with logic input voltage levels only.

SIZE	SYMBOL	DRAWING NO.	REV
A	3	C3004NS	A
		SCALE:	SHEET 4 OF 4

NOT SCALE PRINT

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN 3035		16 DEC 69	J.E.H.

REV STATUS OF SHEETS																	
	REV	A	A	A	A	A											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
DRAFTING	J.E.H.	J.E.H.	16 DEC 69
DESIGNED			

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT, INTEGRATED
DUAL IN-LINE PACKAGE
TYPE SN7403N

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED
LOCAL RELEASE J.E.H. 16 DEC 69
CORPORATE RELEASE [illegible] JAN 73

SIZE A | B

DRAWING NUMBER C3004NT

DESIGNED FOR

SCALE

WT

SHEET 1 OF 5

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Quadruple 2-input NAND gate with open collector output.

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheets 4 & 5.

4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7403N

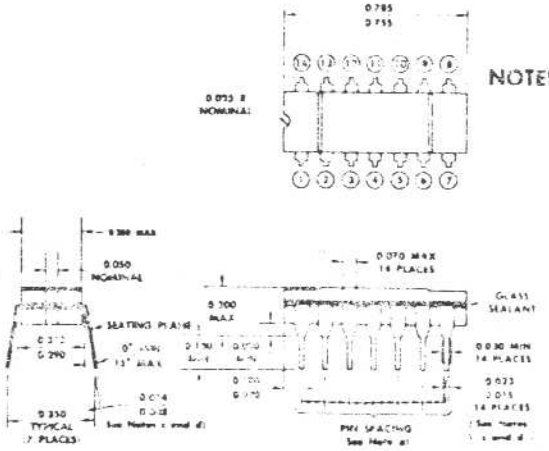
Sprague Part No. USN7403
National Semiconductor Corp. DM8003N

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3004NT	A
		SCALE:	SHEET 2 OF

DO NOT SCALE PRINT

FORM A818-088-4/68



NOTES:
a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (7) and (14).
b. All dimensions in inches unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.
e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

SIZE	SYMBOL	DRAWING NO.	REV
A	B	[illegible]	A

NOT SCALE PRINT

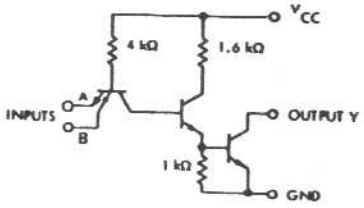
SCALE:

SHEET [illegible] OF

[illegible] 30838 (6/67)

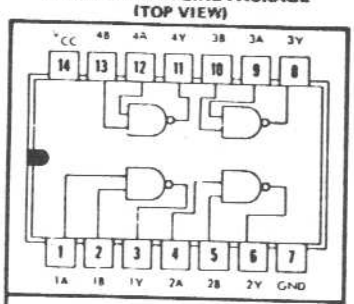
CIRCUIT TYPES SN5403, SN7403
QUADRUPLE 2-INPUT POSITIVE NAND GATES
(WITH OPEN-COLLECTOR OUTPUT)

schematic (each gate)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

SIZE	SYMBOL	DRAWING NO.	REV
A	B	LC3004NT	A
	SCALE:		SHEET 4 OF

DO NOT SCALE PRINT

FORM 50535 (6/67)

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5403 Circuits	4.5	5	5.5	V
SN7403 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 2-7 and 2-8)			10	
Operating Free-Air Temperature Range, T_A: SN5403 Circuits	−55	25	125	°C
SN7403 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output)	1	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7	V_{CC} = MIN, V_{in} = 0.8 V,			0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, V_{in} = 2 V, $V_{out(1)}$ = 5.5 V			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX, V_{in} = 5 V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX, V_{in} = 0		4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 4 kΩ		35	45	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3004 NT	A
SCALE:		SHEET 5 OF 5	

DO NOT SCALE PRINT

SN 5083B (6/67)

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN 3035		16 DEC 69	JOHN HATCH
B	REVISED & REDRAWN PER ECN 4398		22 JAN 73	W. J. J.

REV																			
SHEET																			
REV																			
SHEET	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50				
REV																			
SHEET	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
REV STATUS OF SHEETS	REV		B	B	B	B													
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

DRAWN J.E.H	CHK'D J.E.H	DATE 16 DEC 72
DRAFTING		
DESIGNED		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A

TITLE
Purchase Spec.
Integrated Circuit Dual In-Line Pkg.
Type SN7404N

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED	
LOCAL RELEASE	
CORPORATE RELEASE B. FRANKLIN	1/11/73

SIZE		DRAWING NUMBER
A	B	C3004NW

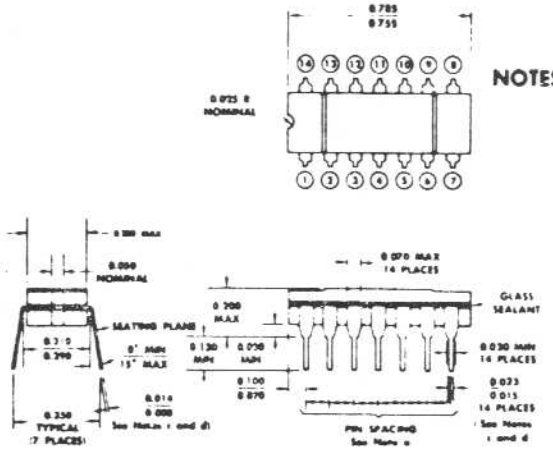
DESIGNED FOR

SCALE

WT

SHEET 1 OF 4

FORM 5758-A (5/69)



NOTES:
a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)
b. All dimensions in inches unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.
e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

FIG. 1

SIZE	SYMBOL	DRAWING NO.	REV
A	B	EC3004NW	B
SCALE:		SHEET 2 OF	

DO NOT SCALE PRINT

FORM 50838 (6/67)

1.0 DESCRIPTION

Circuit, Integrated (Dual In-Line Pkg. hex inverter)

2.0 REQUIREMENTS

2.1 Electrical: See Table 1 (Sheet 4)

2.2 Mechanical: See Figure 1 (Sheet 2)

3.0 VENDOR

Texas Instrument Part No. SN7404N

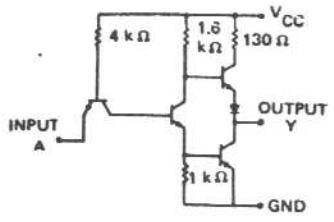
Sprague Part No. USN7404

Motorola Part No. MC7404P

National Semiconductor Corp. Part No. DM8004N

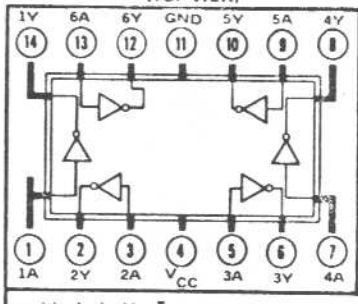
TABLE 1

schematic (each inverter)

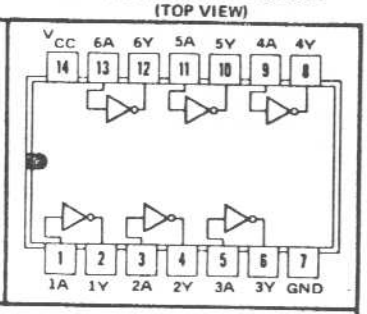


NOTE: Component values shown are nominal

S FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \bar{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5404 Circuits	4.5	5	5.5	V
SN7404 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N			10	
Operating Free-Air Temperature Range, T_A: SN5404 Circuits	−55	25	125	°C
SN7404 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 level at output	15	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	16	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	16	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	15	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each Logical 0 level input current	17	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current	18	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	19	V_{CC} = MAX	SN5404	−20		−55	mA
				SN7404	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	20	V_{CC} = MAX, V_{in} = 5 V			18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	20	V_{CC} = MAX, V_{in} = 0			6	12	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω			8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω			12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

REVISIONS				
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	ISSUED ECN NO. 3070		15 JAN 70	J. E. H

REV STATUS OF SHEETS	REV	A	A	A	A	A											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

DRAWN A.ZIKAS	CHK'D	DATE 11/4/69	
DRAFTING			
DESIGNED			

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT, INTEGRATED
DUAL IN-LINE PACKAGE
TYPE SN74121

SUPERSEDING INTERCHANGEABLE SIMILAR TO YES NO	APPROVED		
	LOCAL RELEASE J. HATCH	15 JAN 70	
DESIGNED FOR	CORPORATE RELEASE B. FRANKLIN	5 JUNE	

SIZE		DRAWING NUMBER
A	B	C3004PL
SCALE	WT	SHEET 1 OF 5

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual in-line package) mono stable multivibrator.

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 4.

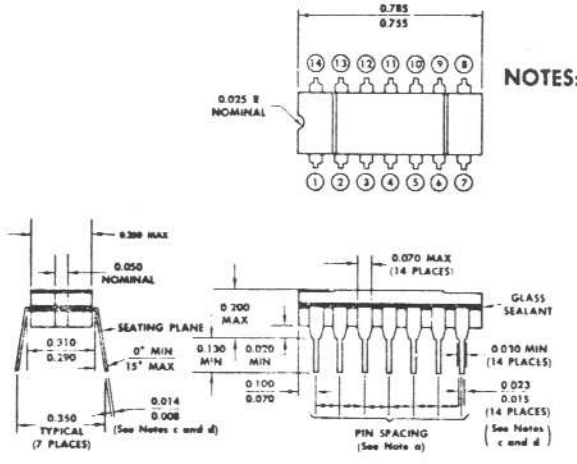
4. MANUFACTURER'S NAME AND PART NO.

Texas Instruments Part No. SN74121

SIZE	SYMBOL	DRAWING NO.	REV
A		C3004PL	A
		SCALE:	SHEET 1 OF

DO NOT SCALE PRINT

FORM A816-088-4/68



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

CIRCUIT TYPES SN54121, SN74121
MONOSTABLE MULTIVIBRATORS

logic

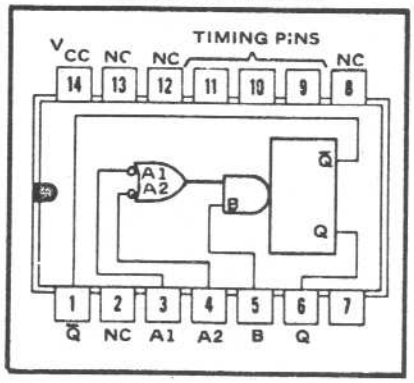
TRUTH TABLE (See Notes 1 thru 3)

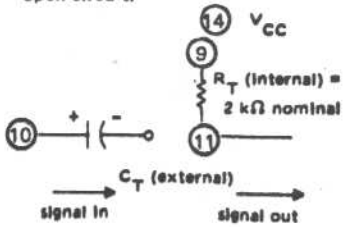
t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

$1 = V_{in(1)} \geq 2\ V$
$0 = V_{in(0)} \leq 0.8\ V$

NOTES:
1. t_n = time before input transition.
2. t_{n+1} = time after input transition.
3. X indicates that either a logical 0 or 1, may be present.
4. NC = No Internal Connection.
5. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
6. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)
7. External timing capacitor may be connected between pin (10) (positive) and pin (11). With no external capacitance, an output pulse width of typically 30 ns is obtained.
8. To use the internal timing resistor (2 kΩ nominal), connect pin (9) to pin (14).
9. To obtain variable pulse width connect external variable resistance between pin (9) and pin (14). No external current limiting is needed.
10. For accurate repeatable pulse widths connect an external resistor between pin (11) and pin (14) with pin (9) open-circuit.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)
(SEE NOTES 6 THRU 9)





SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3004PL	A
SCALE:		SHEET 4 OF	

NOT SCALE PRINT

electrical characteristics over operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNITS
V_{T+}	Positive-going threshold voltage at A input	57	V_{CC} = MIN			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	57	V_{CC} = MIN		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	57	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	57	V_{CC} = MIN		0.8	1.35		V
$V_{out(0)}$	Logical 0 output voltage	57	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$V_{out(1)}$	Logical 1 output voltage	57	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.3		V
$I_{in(0)}$	Logical 0 level input current at A1 or A2	58	V_{CC} = MAX, V_{in} = 0.4 V			−1	−1.6	mA
$I_{in(0)}$	Logical 0 level input current at B	59	V_{CC} = MAX, V_{in} = 0.4 V			−2	−3.2	mA
$I_{in(1)}$	Logical 1 level input current at A1 or A2	60	V_{CC} = MAX, V_{in} = 2.4 V			2	40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			0.05	1	mA
$I_{in(1)}$	Logical 1 level input current at B	61	V_{CC} = MAX, V_{in} = 2.4 V			4	80	μA
			V_{CC} = MAX, V_{in} = 5.5 V			0.05	1	mA
I_{OS}	Short circuit output current at Q or $\overline{Q}$§	62 and 63	V_{CC} = MAX	SN54121	−20	−25	−55	mA
				SN74121	−18	−25	−55	
I_{CC}	Power supply current in quiescent (unfired) state	64	V_{CC} = MAX			13	25	mA
I_{CC}	Power supply current in fired state	64	V_{CC} = MAX			23	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd1}	Propagation delay time to logical 1 level from B input to Q output	72	C_L = 15 pF,	C_T = 80 pF	15	35	55	ns
t_{pd1}	Propagation delay time to logical 1 level from A1/A2 inputs to Q output				25	45	70	ns
t_{pd0}	Propagation delay time to logical 0 level from B input to $\overline{Q}$ output	72	C_L = 15 pF,	C_T = 80 pF	20	40	65	ns
t_{pd0}	Propagation delay time to logical 0 level from A1/A2 inputs to $\overline{Q}$ output				30	50	80	ns
$t_{p(out)}$	Pulse width obtained using internal timing resistor	73	C_L = 15 pF, R_T = Open,	C_T = 80 pF, Pin ⑨ to V_{CC}	70	110	150	ns
$t_{p(out)}$	Pulse width obtained with zero timing capacitance	73	C_L = 15 pF, R_T = Open,	C_T = 0, Pin ⑨ to V_{CC}	20	30	50	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	73	C_L = 15 pF, R_T = 10 kΩ,	C_T = 100 pF, Pin ⑨ Open	600	700	800	ns
			C_L = 15 pF, R_T = 10 kΩ,	C_T = 1 μF, Pin ⑨ Open	6	7	8	ms
t_{hold}	Minimum duration of trigger pulse	73	C_L = 15 pF, R_T = Open,	C_T = 80 pF, Pin ⑨ to V_{CC}		30	50	ns

REVISIONS				
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
B	ECN NO. 3919		23/JUN 71	W. T.

REV STATUS OF SHEETS	REV	B	B	B	B	B	B										
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

DRAWN B. WHITE	CHK'D	DATE 4/1/71
DRAFTING		
DESIGNED		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT, INTEGRATED
DUAL IN-LINE PACKAGE
TYPE SN7405LJ

SUPERSEDING INTERCHANGEABLE SIMILAR TO YES NO	APPROVED	SIZE A	B
	LOCAL RELEASE J. CLARK		
DESIGNED FOR	CORPORATE RELEASE B. FRANKLIN 4 JUN 73	SCALE	WT

DRAWING NUMBER C3007MR

SHEET 1 OF 6

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Hex Inverters (with open collector output)

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5.

4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7405N
Sprague Part No. USN7405A
Motorola Part No. MC7405P

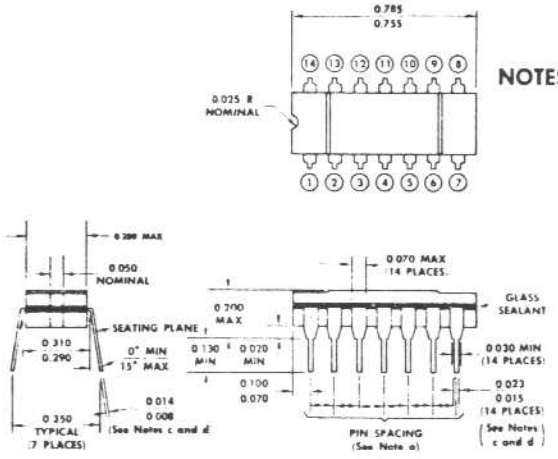
NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3007MR	B

DO NOT SCALE PRINT

SCALE:

SHEET 2 OF



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

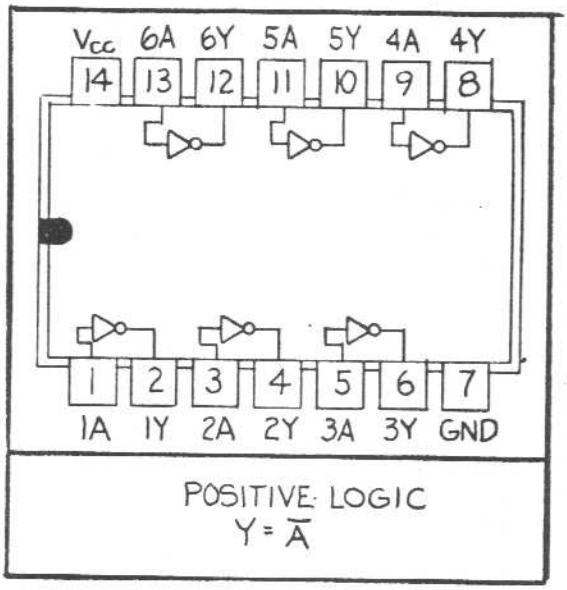
c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

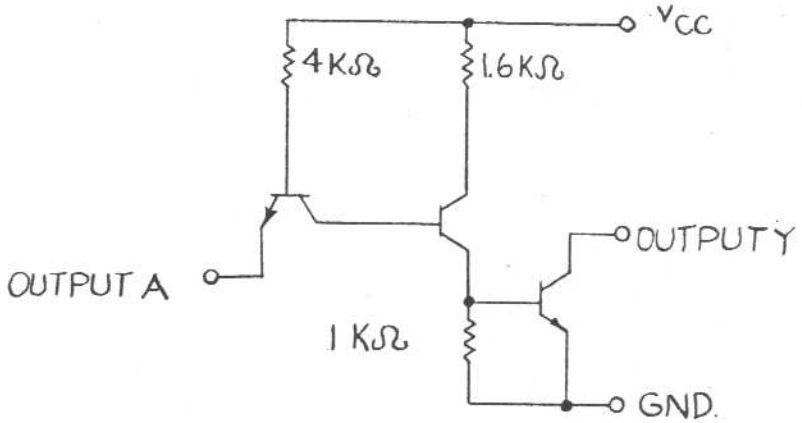
14-PIN FUNCTIONS

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



POSITIVE LOGIC
$Y = \overline{A}$

SCHEMATIC (EACH GATE)



SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3007MR	B
SCALE:		SHEET 1 OF	

DO NOT SCALE PRINT

FORM 50838 (6/67)

FORM 5083B (6/67)

DO NOT SCALE PRINT

RECOMMENDED OPERATING CONDITIONS
SUPPLY VOLTAGE - 4.75 - 5.25 V

ELECTRICAL CHARACTERISTICS (OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE)

PARAMETER	TEST FIGURE	TEST CONDITIONS †	MIN. - TYP.# MAX	UNIT
$V_{IN(1)}$ LOGICAL 1 INPUT VOLTAGE REQ'D AT INPUT TERMINAL TO ENSURE LOGICAL 1 (OFF) LEVEL AT OUTPUT	15	V_{CC} = MIN.	2	V
LOGICAL 0 INPUT VOLTAGE REQ'D. AT INPUT TERMINAL TO ENSURE LOGICAL 1 (OFF) LEVEL AT OUTPUT.	16	V_{CC} = MIN.	0.8	V
$I_{OUT(1)}$ OUTPUT REVERSE CURRENT	16	V_{CC} = MIN, V_{IN} = 0.8V, $V_{OUT(1)}$ = 5.5V	250	μA
$V_{OUT(0)}$ LOGICAL 0 OUTPUT VOLTAGE (ON LEVEL)	15	V_{CC} = MIN, V_{IN} = 2V, I_{SINK} = 16 mA	0.4	V
$I_{IN(0)}$ LOGICAL 0 LEVEL INPUT CURRENT	17	V_{CC} = MAX, V_{IN} = 0.4V	-1.6	mA
$I_{IN(1)}$ LOGICAL 1 LEVEL INPUT CURRENT	18	V_{CC} = MAX, V_{IN} = 2.4 V	40	μA
		V_{CC} = MAX, V_{IN} = 5.5 V	1	mA
$I_{CC(0)}$ LOGICAL 0 LEVEL SUPPLY CURRENT	20	V_{CC} = 5V, V_{IN} = 5V, T_A = 25°C	18 33	mA
$I_{CC(1)}$ LOGICAL 1 LEVEL SUPPLY CURRENT	20	V_{CC} = 5V, V_{IN} = 0, T_A = 25°C	6 12	mA

NOTES:
1. † FOR CONDITIONS SHOWN AS MIN OR MAX, USE THE APPROPRIATE VALUE SPECIFIED UNDER RECOMMENDED OPERATING CONDITIONS FOR THE APPLICABLE DEVICE TYPE.
2. # THESE TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3007 MR	B

SCALE: none

SHEET 5 OF

DO NOT SCALE PRINT

FORM 5083B (6/67)

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN.	TYP	MAX	UNIT
$T_{PD\emptyset}$ PROPAGATION DELAY TIME TO LOGICAL Ø LEVEL	65	$C_L = 15PF$, $R_L = 400\Omega$		8	15	NS
T_{PD1} PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL.	65	$C_L = 15PF$, $R_L = 4\Omega$		40	55	NS

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3007MR	3

SCALE: 4/1

SHEET 6 OF 6

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN. 3146		11 MAR 70	J.E.H.

FIRST USED ON:
C 3001 XX

REV STATUS OF SHEETS																	
REV	A	A	A	A	A	A											
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

DRAWN S. WALKER | CHK'D | DATE 15 MAR 70
DRAFTING
DESIGNED

FOXBORO
THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
Circuit, Integrated
Dual In-Line Package Type SN74107

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED
LOCAL RELEASE J. HATCH | 11 MAR 70

SIZE A | B

DRAWING NUMBER
C3008BZ

DESIGNED FOR

CORPORATE RELEASE B. FRANKLIN | 27 AUG 73

SCALE | WT | SHEET 1 OF 6

FORM 5758-C (5/69)

1.0 DESCRIPTION:

Circuit, Integrated (Dual In-Line Package)
Dual J-K Master-Slave Flip-Flops

2.0 PHYSICAL CHARACTERISTICS:

2.1 See Sheet 3.

3.0 PERFORMANCE CHARACTERISTICS:

3.1 See Sheet 5.

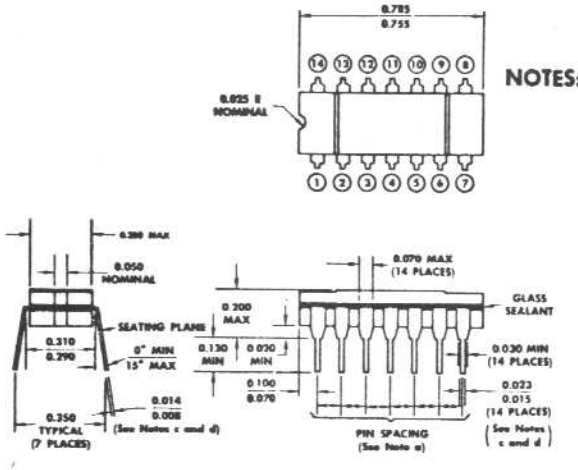
4.0 MANUFACTURER'S NAME AND PART NO.:

Texas Instrument, Part No. SN74107

Note: Only the item descibed on this drawing when procurred from the manufacturèrs listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3008BZ	A
DO NOT SCALE PRINT	SCALE:	SHEET 2 OF 6	

FORM A816-888-4/68



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

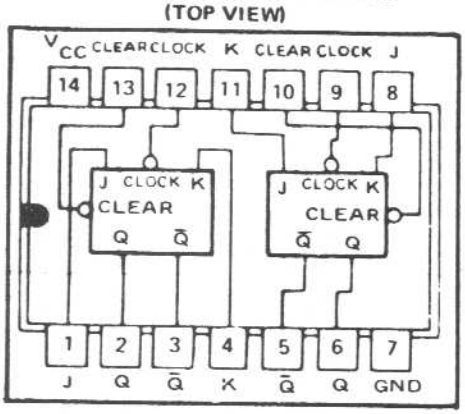
c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

SN74107
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Low input to clear sets Q to logical 0.
Clear is independent of clock.

description

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: (See waveform on page 2-26)

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

logic

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

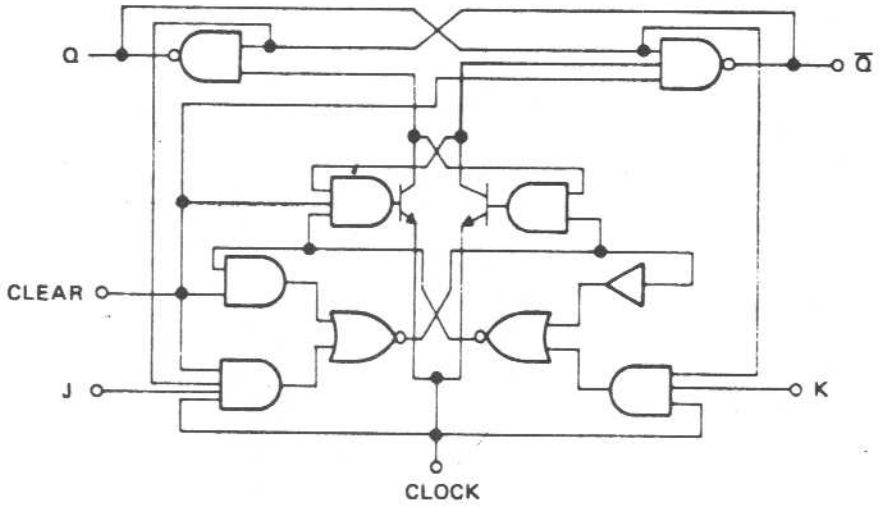
recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5473, SN54107 Circuits	4.5	5	5.5	V
	SN7473, SN74107 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A:		-55	25	125	°C
	SN74107 Circuits	0	25	70	°C
Normalized Fan-Out From Eacn Output, N				10	
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 69)		20			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 70)		25			ns
Input Setup Time, t_{setup} (See Figure 69)		$\geq t_{p(clock)}$			
Input Hold Time, t_{hold}		0			

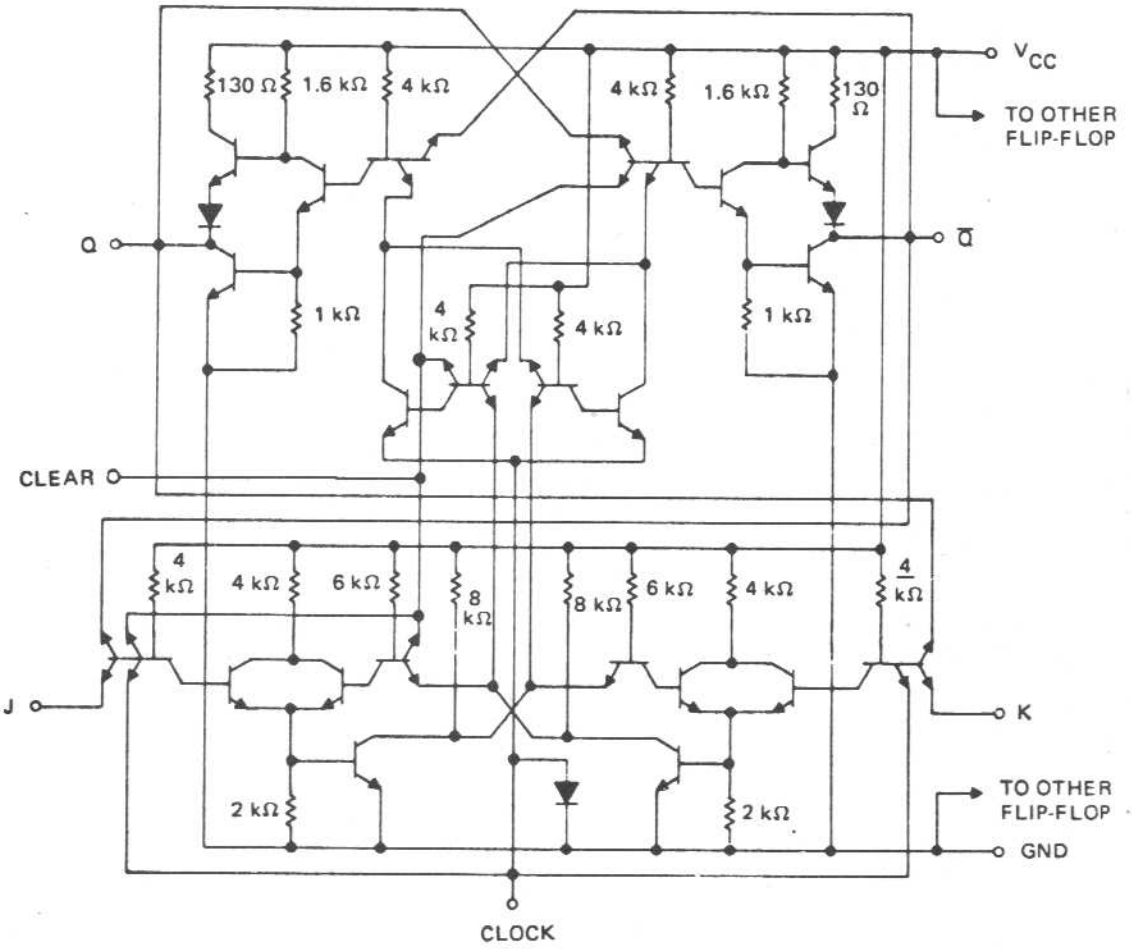
SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3008BZ	A
SCALE:		SHEET 4 OF 6	

DO NOT SCALE PRINT

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3008BZ	A

DO NOT SCALE PRINT

SCALE:

SHEET 5 OF 6

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	46 and 47	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	46 and 47	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	46	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	47	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	48	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	48	V_{CC} = MAX,	V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	49	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear or clock	49	V_{CC} = MAX,	V_{in} = 2.4 V				80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	50	V_{CC} = MAX,	V_{in} = 0	SN5473, SN54107	−20		−57	mA
					SN7473, SN74107	−18		−57	
I_{CC}	Supply current	49	V_{CC} = MAX,	V_{in} = 5 V			20	40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	69	C_L = 15 pF,	R_L = 400 Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	70	C_L = 15 pF,	R_L = 400 Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	70	C_L = 15 pF,	R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	25	40	ns

REVISIONS				
LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN 3203		3/8/70	M.J.C

REV STATUS OF SHEETS																	
REV	A	A															
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

DRAWN H. McEvoy | CHK'D | DATE 3/3/70
DRAFTING
DESIGNED

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT, INTEGRATED
DUAL IN-LINE PACKAGE
TYPE SN7442

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED
LOCAL RELEASE M. COOK 4/15/70
CORPORATE RELEASE E. FRANKLIN 4/20/70

SIZE A | B

DRAWING NUMBER C3008FL

DESIGNED FOR

SCALE | WT | SHEET 1 OF 2

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated
4 line to 10 line decoder

2. PHYSICAL CHARACTERISTICS

2.1 16 pin dual in-line package.

For more detailed physical characteristics, see mfg.'s catalog.

3. PERFORMANCE CHARACTERISTICS

3.1 Supply voltage Vcc - 4.75V to 5.25V
3.2 Fan out - 10 unit loads
3.3 Ambient temperature - 0°C to 70°C

For more detailed performance characteristics, see mfg.'s catalog.

4. QUALITY ASSURANCE PROVISIONS

Inspect per parameter outlined in mfg.'s catalog.

5. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, or Engineering approved equivalent.

Part No. SN7442

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3009FL	A
		SCALE:	SHEET 2 OF 2

DO NOT SCALE PRINT

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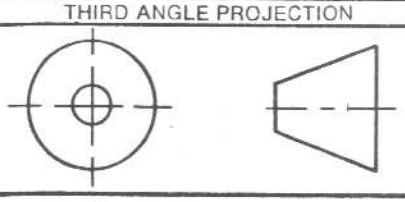
THIRD ANGLE PROJECTION



REVISIONS

SYM	CHANGE NO.	DATE	APP
A	3377 N	7/15/70	RMJ

FIRST USED ON APPLICATION

GR

DO NOT SCALE DRAWING

DESCRIPTION

Dual J-K Flip Flop DTML

PHYSICAL CHARACTERISTICS

Dual in Line, 14 PIN

PERFORMANCE CHARACTERISTICS

For detail specification see mfg. catalog

QUALITY ASSURANCE PROVISIONS

Inspect per this drawing

MANUFACTURERS NAME AND PARTNUMBER

Fairchild Semiconductor P/N 9093
Mountain View, California

PRINT DISTR DEPT	QTY

FOR PARTS LIST SEE DWG PL

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

.X ± | .XX ±.04 | .XXX ±.010

NGLES ± FRACTIONS ± | ⊕ .028 DIA

MATL

FINISH

DRAWN		DATE
CHECKED		
DESIGNED RMJ		5/22/70
DRAFTING		
RESTRICTED RELEASE		
LOCAL RELEASE RMJ		7/15/70
CORPORATE RELEASE		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
PURCHASE SPECIFICATION
I.C. Package, Dual In-Line
Type 9093

SIZE	DWG CODE		DRAWING NUMBER	REV
A		B	C3009SM	A

SCALE | WT | SHEET 1 OF 1

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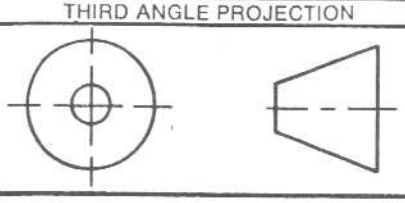
THIRD ANGLE PROJECTION



REVISIONS	SYM	CHANGE NO.	DATE	APP
	A	3377	7/15/70	RM

FIRST USED ON APPLICATION

GR

DO NOT SCALE DRAWING

DESCRIPTION

Buffer Storage Elements, C_m 1

PHYSICAL CHARACTERISTICS

Dual in Line, 16 Pin

PERFORMANCE CHARACTERISTICS

For Detailed Specifications see Mfg. Catalog

QUALITY ASSURANCE PROVISIONS

Inspect per this Drawing

MANUFACTURER'S NAME AND PART NUMBER

Fairchild Semiconductor P/N 9959
Mountain View, Cal.

PRINT DISTR DEPT	QTY

FOR PARTS LIST SEE DWG PL

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

.X ± | .XX ±.04 | .XXX ±.010

NGLES ± FRACTIONS ± | ⊕ .028 DIA

MATL

FINISH

DRAWN		DATE
CHECKED		
DESIGNED	RM	5/22/70
DRAFTING		
RESTRICTED RELEASE		
LOCAL RELEASE	RM	7/15/70
CORPORATE RELEASE		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE: PURCHASE SPECIFICATION
I.C. Package, Dual In-Line
Type 9959

SIZE	DWG CODE	DRAWING NUMBER	REV
A	B	C3009SS	A

SCALE | WT | SHEET 1 OF 1

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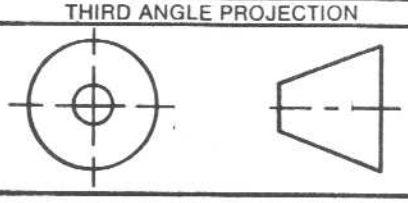
THIRD ANGLE PROJECTION



REVISIONS

SYM	CHANGE NO.	DATE	APP
A	LOCAL RELEASE ECN 3459	9/23/70	RH

C3001XX

FIRST USED ON APPLICATION GR

DO NOT SCALE DRAWING

DESCRIPTION

Nixie Decoder/Driver

One out of ten decoder

PHYSICAL CHARACTERISTICS

16 Pin Dual In-Line Package

PERFORMANCE CHARACTERISTICS

Operating Temperature Range 0°C to 75°C

VCC. = 5V ± 5%

"1" Output Voltage 68V min, "1" input current 25ma

"0" Output Voltage 2.75 max, "0" input current (1 & 8 - .9ma) (2 & 4 - 1.8ma) max.

PRINT DISTR DEPT	QTY

QUALITY ASSURANCE PROVISIONS

Inspect per this drawing

MANUFACTURERS NAME AND PART NUMBER

Signetics Corporation
Sunnyvale, Calif.

#N8T01B NOTE: Engineering approved equivalent may be used.

FOR PARTS LIST SEE DWG PL

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

.X ± | .XX ±.04 | .XXX ±.010

ANGLES ± FRACTIONS ± | ⊕ .028 DIA

MATL

FINISH

		DATE
DRAWN		
CHECKED		
DESIGNED	E Heberle	9/23/70
DRAFTING		
RESTRICTED RELEASE		
LOCAL RELEASE	[illegible]	9/23/70
CORPORATE RELEASE		

FOXBORO THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.

TITLE

PURCHASE SPECIFICATION

IC Package Signetic N8T01B

SIZE	DWG CODE		DRAWING NUMBER	REV
A		B	C3009ST	H

SCALE | WT | SHEET 1 OF 1

FORM 5877 [11/69]

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN # 4057 M		2/13/72	[illegible]

REV STATUS OF SHEETS																	
REV	A						A										
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
DRAFTING			
DESIGNED	[illegible]		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE

DUAL-IN-LINE PACKAGE I.C. DEC TYPE 380A

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED	[illegible]	
LOCAL RELEASE	[illegible]	
CORPORATE RELEASE	B. FRANKLIN	2/28/72

DESIGNED FOR FOX-2

SIZE		DRAWING NUMBER
A	B	C3313AA

SCALE	WT	SHEET 1 OF 7

FORM 5758-C (5/69)

DESCRIPTION Dual-In-Line Package, I.C. DEC Type 380A

QUAD, 2 Input-Nor

PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin (See sheet #3
Must withstand soldering temperature with no deformation.

PERFORMANCE CHARACTERISTICS

Supply Voltage: 5.5 Volts Continuous (see note 1)
Input Voltage: 5.5 Volts (see note 1 and 2)
Recommended Operating Conditions: 4.75 to 5.25 Volts
Storage Temperature Range: - 55°C to 125°C

Notes: 1. Voltage values are with respect to network ground terminal.

2. Input signals must be zero or positive with respect to network ground terminal.

QUALITY ASSURANCE PROVISIONS

Inspect per this drawing.

MANUFACTURER'S NAME AND PART NUMBER

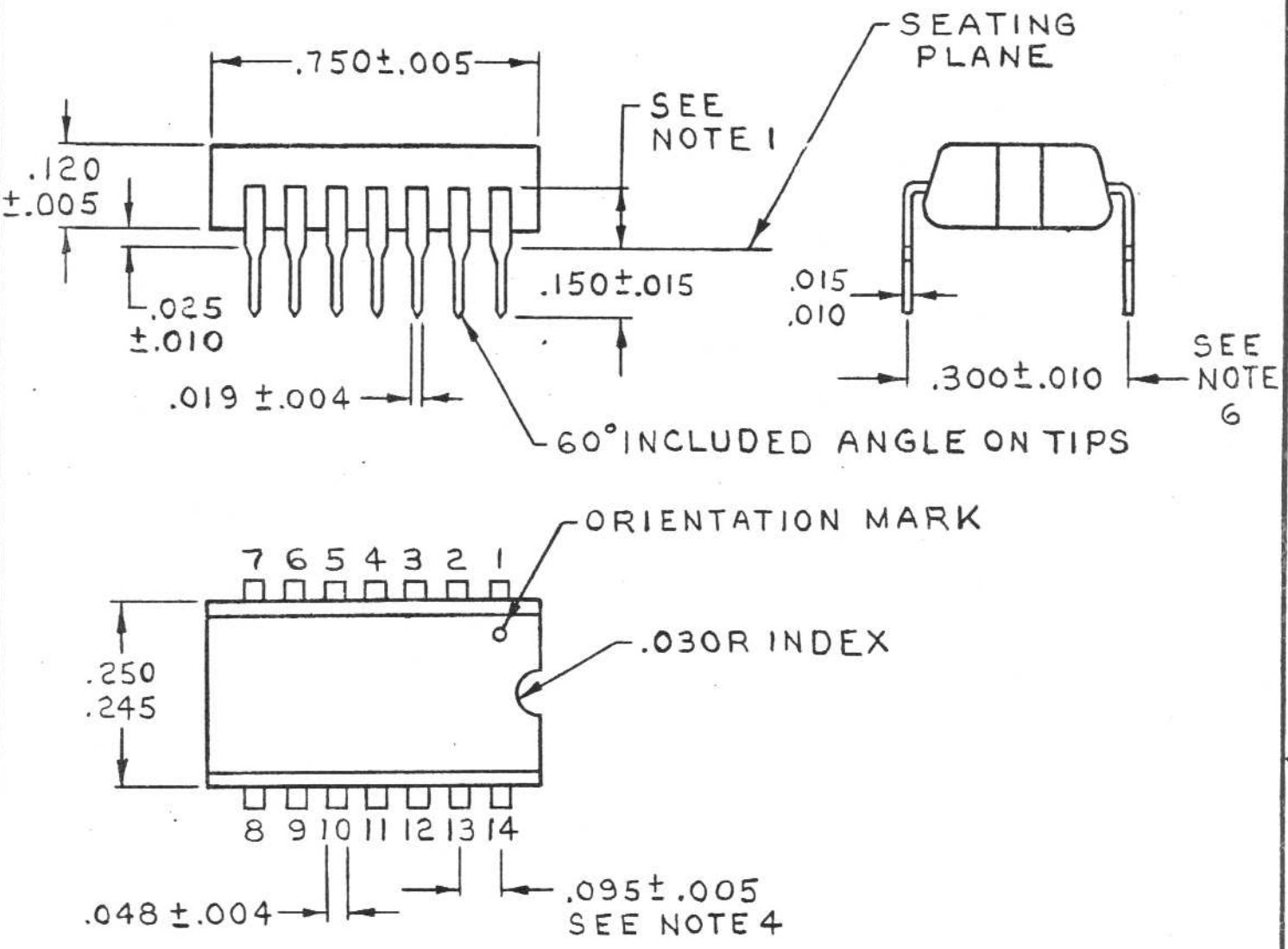
Digital Equipment Corporation
146 Main Street
Maynard, Mass. P/N 19-09705 (DEC TYPE 380A

OR EQUIVALENT FROM QUALIFIED VENDOR
WHO MEETS SPECIFICATIONS

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AA	A
		SCALE:	SHEET 2 OF

DO NOT SCALE PRINT

FORM A816-0BB-4/66



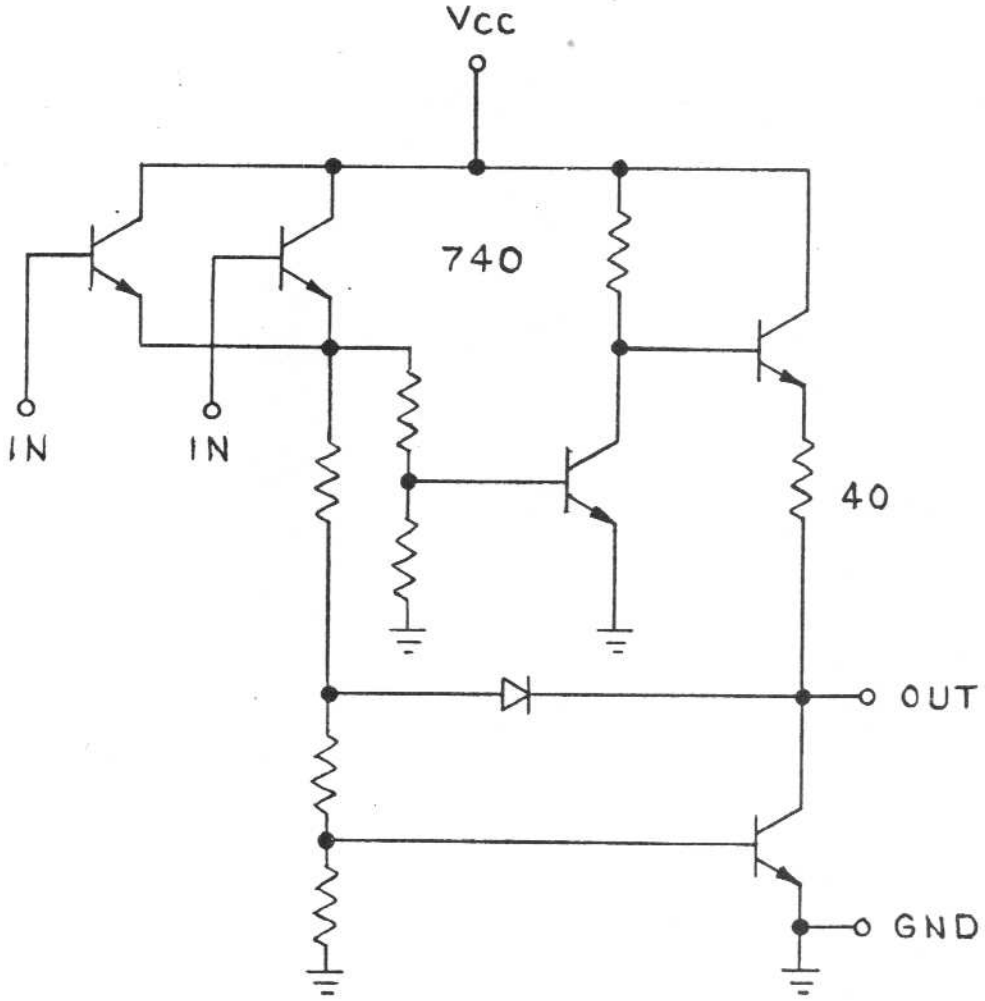
NOTES:

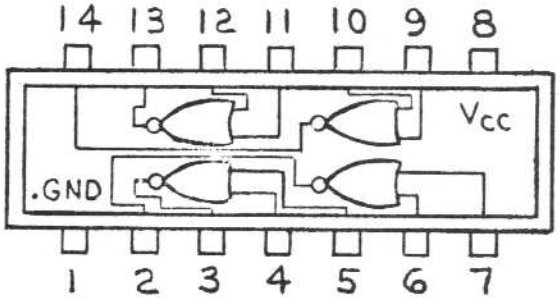
1. Lead spacing shall be measured within this zone.
2. Molded plastic body.
3. Kovar Leads
4. Lead spacing tolerances are non-cumulative
5. Thermal resistance from junction to still air, θ_{J-A}=0.16° C/MW
6. Dimensions while inserted in carrier per DEC SPEC 19 00000 00

SIZE	SYMBOL	DRAWING NO.	REV.
A	B	C3313AA	A
DO NOT SCALE PRINT	SCALE:	SHEET 3 OF	

FORM A816-0BB-4/68

CIRCUIT SCHEMATIC
($\frac{1}{4}$ OF CIRCUIT SHOWN)



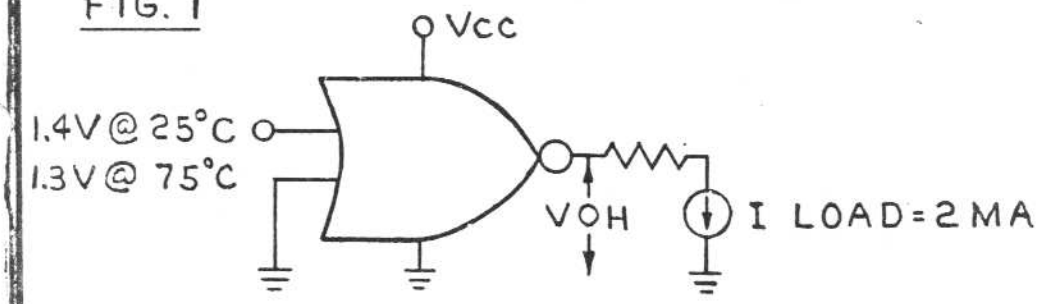


SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AA	A
SCALE:		SHEET 4 F	

DO NOT SCALE PRINT

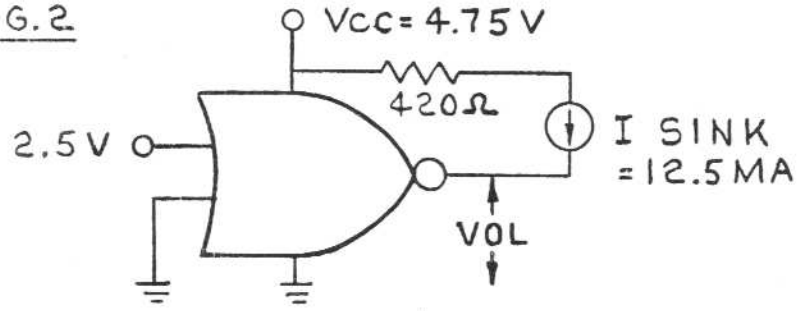
FORM A816-088-4/88

FIG. 1



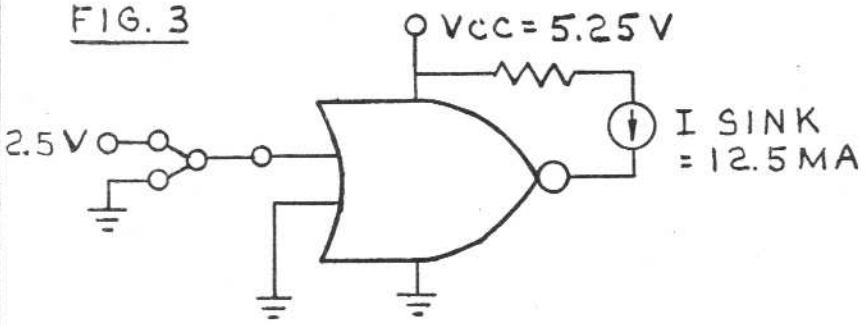
1. EACH INPUT TESTED SEPARATELY

FIG. 2



2. EACH INPUT TESTED SEPARATELY

FIG. 3



3. EACH INPUT TESTED SEPARATELY

FIG. 4

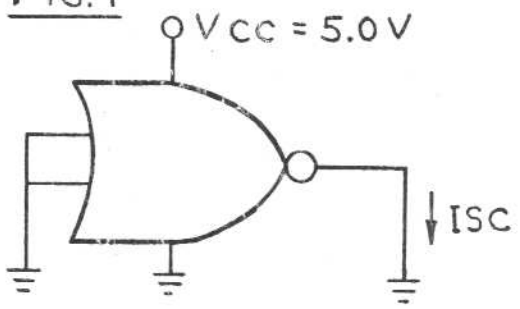
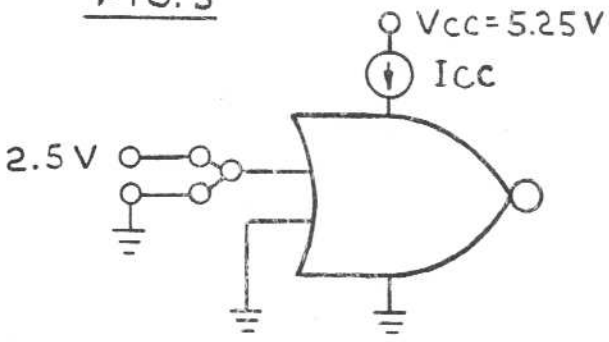


FIG. 5



TEST ALL FOUR GATES SIMULTANEOUSLY

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AA	A
DO NOT SCALE PRINT	SCALE:		SHEET 6 OF

FORM A816-088-4/68

DO NOT SCALE PRINT

FORM A816-0888-4/88

ELECTRICAL CHARACTERISTICS, T_A=0°C to 75°C					
PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN.	MAX.	UNIT
1. V_{OH} Output High Voltage	1	V_{CC}: 4.75 V	3.5		V
2. V_{OL} Output Low Voltage	2	V_{CC}: 4.75 V		0.6	V
3. V_{IH} Input High Voltage	2	V_{CC}: 4.75 V	2.5		V
4. V_{IL} Input Low Voltage	1	V_{CC}: 5.25 V		1.4@ 25°C 1.3@ 75°C	V
5. I_{IH} Input High Current	3	V_{CC}: 5.25 V		160	µA
6. I_{IL} Input Low Current	3	V_{CC}: 5.25 V		-25	µA
7. I_{SC} Output Short Circuit Current	4	V_{CC}: 5.0 V	-30	-100	MA
8. I_{CC} Supply Current (V_{IL})	5	V_{CC}: 5.25 V		2	MA
9. I_{CC} Supply Current (V_{IH})	5	V_{CC}: 5.25 V		50	MA
SHALL BE CAPABLE OF MEETING SWITCHING CHARACTERISTICS, T_A = 0°C to 75°C					
10. TPD 0 Positive Trigger Input TO Output Leading Edge	6	V_{CC}: 5.0 V CL: 15 PF CL: 50 PF	 10 10	 35 45	 NS NS
11. TPD 1 Negative Trigger Input TO Output Trailing Edge	6	V_{CC}: 5.0 V CL: 15 PF CL: 50 PF	 10 10	 45 50	 NS NS

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AA	

SCALE:

SHEET 7 OF 7

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN # 4057		2/13/72	WJ/Cook

REV STATUS OF SHEETS																	
REV	A					A											
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
DRAFTING			
DESIGNED	E. M. [illegible]		2/71
APPROVED	WJ/Cook		9/30/71
LOCAL RELEASE	WJ/Cook		2/13/72
CORPORATE RELEASE	B. FRANKLIN		6/28/72

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE

DUAL-IN-LINE PACKAGE I.C. DEC TYPE 8881

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

DESIGNED FOR FOX-2

SIZE		DRAWING NUMBER
A	B	C3313AB

SCALE | WT | SHEET 1 OF 6

FORM 5758-C (5/69)

DESCRIPTION Dual-In-Line Package I. C. DEC Type 8881

QUAD, 2 Input Nand, Open Collector.

PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin (See sheet #3)
Must withstand soldering temperature with no deformation,

PERFORMANCE CHARACTERISTICS

Supply Voltage: 7 Volts (see note 1)
Input Voltage: 5.5 Volts(see note 1 and 2)
Recommended Operating Condition: 4.75 Min. to 5.25 Volts Max.
Operating Free-air Temperature Range: 0°C to 70°C
Storage Temperature Range: - 55°C to 125°C

Note 1. Voltage values are with respect to network ground terminal.

2. Input signals must be zero or positive with respect to network ground terminal.

QUALITY ASSURANCE PROVISIONS:

Inspect per this drawing.

MANUFACTURER'S NAME AND PART NUMBER

Digital Equipment Corporation
146 Main Street
Maynard, Mass.

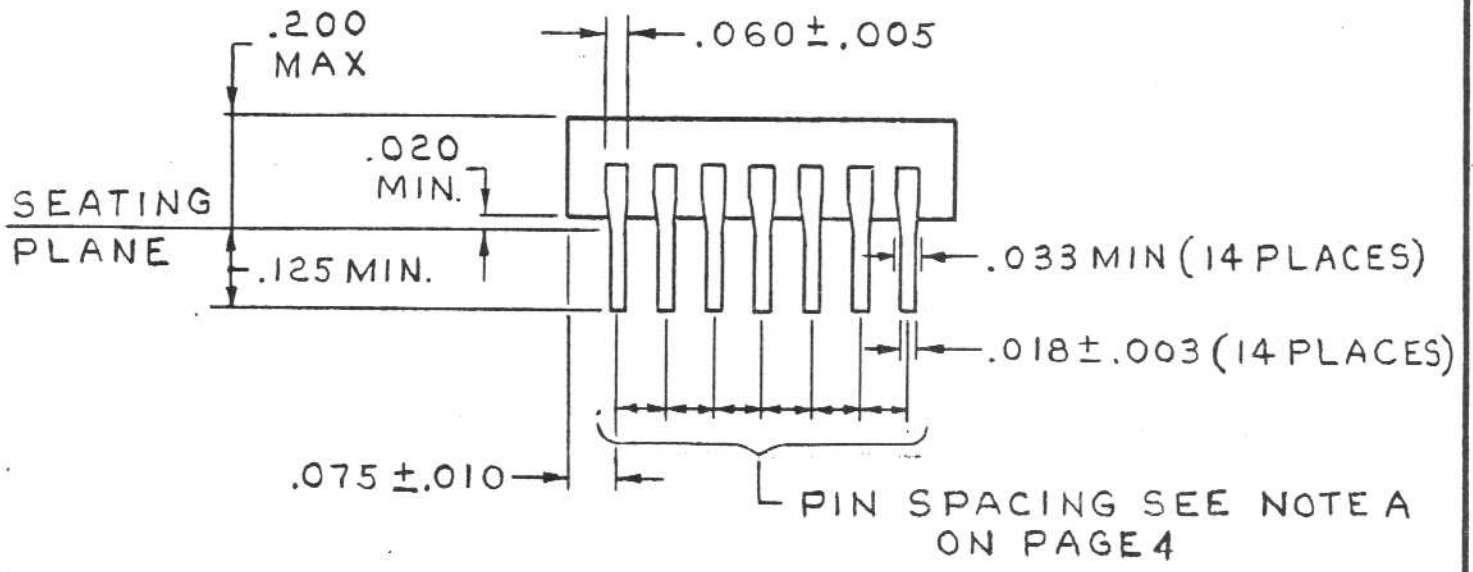
P/N 19-09705 (DEC TYPE 8881

OR EQUIVALENT FROM QUALIFIED VENDOR
WHO MEETS SPECIFICATIONS

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AB	24
		SCALE:	SHEET 2 OF

DO NOT SCALE PRINT

FORM A816-0888-4/68



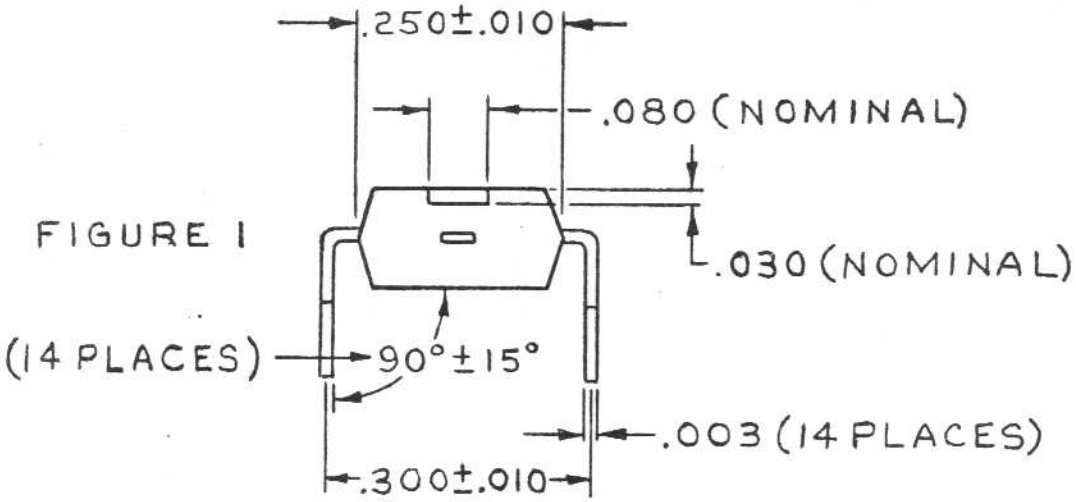
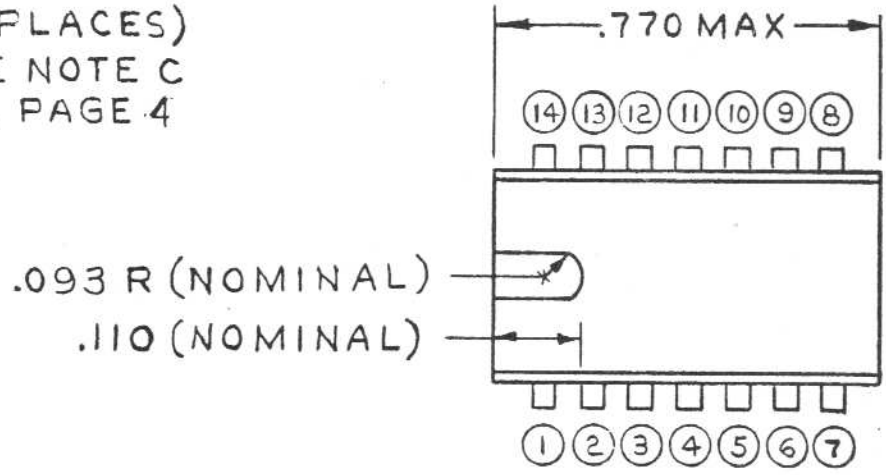


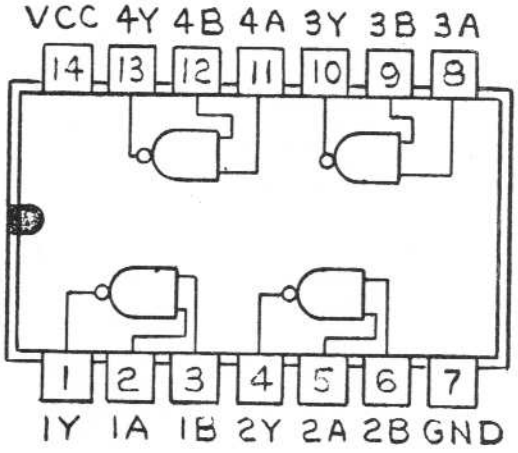
FIGURE 1



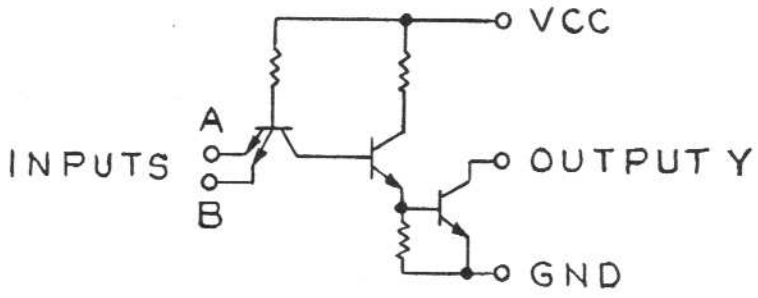
SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AB	A
SCALE:		SHEET 3 OF	

DO NOT SCALE PRINT

FORM A816-0BB-4/68



POSITIVE LOGIC $Y=\overline{AB}$



SCHEMATIC (EACH GATE)

NOTES:

A. The True-position pin spacing is 0.100 between centerlines. Each pin center-line is located within ±0.010 of its true longitudinal position relative to pin 1 and 14.

B. All dimensions in inches unless otherwise noted.

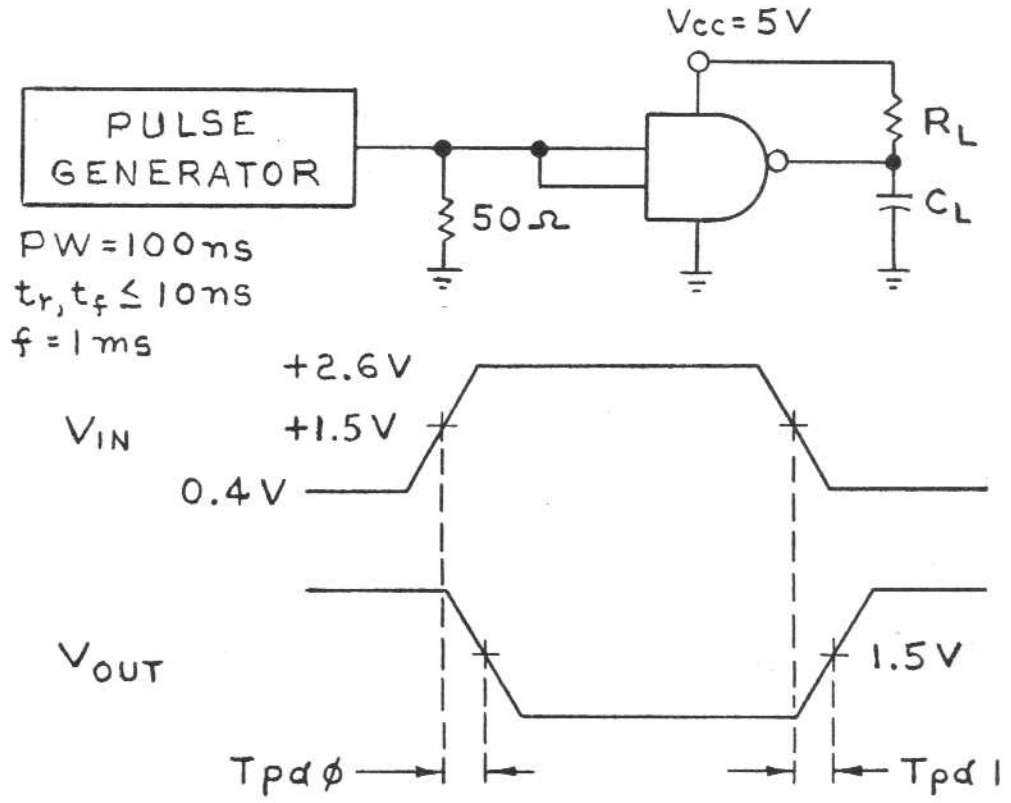
C. Dimensions while inserted in carrier per DEC Spec. 19-00000-00.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AB	A
SCALE:		SHEET 4 OF	

DO NOT SCALE PRINT

FORM A818-0SB-4/68

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C					
PARAMETER	TEST CONDITIONS (Figure 1)	MIN.	TYP.	MAX.	TYPE
$T_{PD\,\emptyset}$ Propagation delay time to logical 0 level	R_L = 100 C_L = 15 PF			25	NS
$T_{PD\,1}$ Propagation delay time to logical 1 level	R_L = 3.9 KIL - OHMS C_L = 15 PF			35	NS



SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AB	A
SCALE:			SHEET 5 OF

DO NOT SCALE PRINT

FORM A816-0BB-4/66

DO NOT SCALE PRINT
FORM A816-0888-4/88

ELECTRICAL CHARACTERISTICS, T_A = 0°C to 70°C					
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
$V_{IN(1)}$ Logical 1 input voltage required at all input terminals to ensure logical 0 (ON) level at output.	V_{CC} = 4.75 V V_{OUT} 0.8 V I_{SINK} = 50 MA	2.0			V
$V_{IN(0)}$ Logical 0 input voltage required at any input terminal to ensure logical 1 (OFF) level at output.	V_{CC} = 4.75 V V_{OUT} (1) = 5.5 V			0.8	V
$I_{OUT(1)}$ Output Reverse Current	V_{CC} = 4.75, V_{IN} = 0.8V V_{OUT} (1) = 3.5 V			25	µA
$V_{OUT(0)}$ Logical 0 output voltage (Test 1)	V_{CC} = 4.75, V_{IN} = 2 V, I_{SINK} = 50 MA			0.8	V
$V_{OUT(0)}$ Logical 0 output voltage (Test 2)	V_{CC} = 4.75, V_{IN} = 2 V, I_{SINK} = 16 MA			0.4	V
I_{IN} (0) Logical 0 Level Input Current Each Input	V_{CC} = 5.25, V_{IN} = 0.4 V			-1.6	MA
I_{CC} (0) Logical 0 Level Supply Current	V_{CC} = 5.25 V, V_{IN} = 5 V			55	MA
I_{CC} (1) Logical 1 Level Supply Current	V_{CC} = 5.25 V, V_{IN} = 0			35	MA

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	Local Release ECN Number 3982		29 OCT 71	RCyT
B	ECN NO. 4102		10 APR 72	RCyT

REV STATUS OF SHEETS																	
REV	A	A	A	A	A	A	—	—	—	—	—	—	—	—	—	—	
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
	PENNA		
DRAFTING			
DESIGNED	E. HEBERT		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
Circuit, Integrated, Dual In-Line Package Type SN 7407,

SUPERSEDING INTERCHANGEABLE SIMILAR TO YES NO	APPROVED		
	LOCAL RELEASE		29 OCT 71
DESIGNED FOR	CORPORATE RELEASE		

SIZE		DRAWING NUMBER
A	B	C3313AC
SCALE	WT	SHEET 1 OF 6

FORM 5758-C (5/69)

1.0 DESCRIPTION

Hex Buffers/Drivers with open-collector, high-voltage outputs.

2.0 PHYSICAL CHARACTERISTICS

14-Pin Plastic Dual-In-Line package (N Type).
Shall be marked with mfg.'s type no.

3.0 PERFORMANCE CHARACTERISTICS

Shall be per Table 1.

4.0 QUALITY ASSURANCE PROVISIONS

Inspect per this drawing.

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texas Instruments, Inc.
Dallas, Texas P/N SN7407

Or Equivalent from qualified vendor who meets specifications.

TABLE 1

RECOMMENDED OPERATING CONDITION

	MIN.	NOM.	MAX.	UNIT
Supply Voltage -VCC	4.75	.5	5.25	V
Output Voltage -VOH			30	V
Low-Level Output Current, IOL			40	MA
Operating free-air temperature range TA	0	25	70	°C

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted).

Parameter	Test Conditions *	MIN.	MAX.	UNIT
VIH-High-Level Input Voltage		2		V
VIL-Low-Level Input Voltage			0.8	V
IOH High-Level Output Current	VCC=MIN VI-2V VOH=MAX		250	UA
VOL Low-Level Output Voltage	VCC=MIN.VI=0.8V IOL=16MA		0.4	V
IIH High-Level Input Current (Each Input)	VCC=MAX.VI=2.4V		40	UA
	VCC=MAX.VI=5.5V		1	MA
IIH Low-Level Input Current (Each Input)	VCC=MAX.VI=0.4V		-1.6	MA
ICCH Supply Current, High-Level Output	VCC=MAX.VI=0	TYP** 29	41	MA
ICCL Supply Current, Low-Level Output	VCC=MAX.VI=0	TYP** 21	30	MA

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AC	B

DO NOT SCALE PRINT

SCALE:

SHEET 3 OF 6

FORM 5083B (6/67)

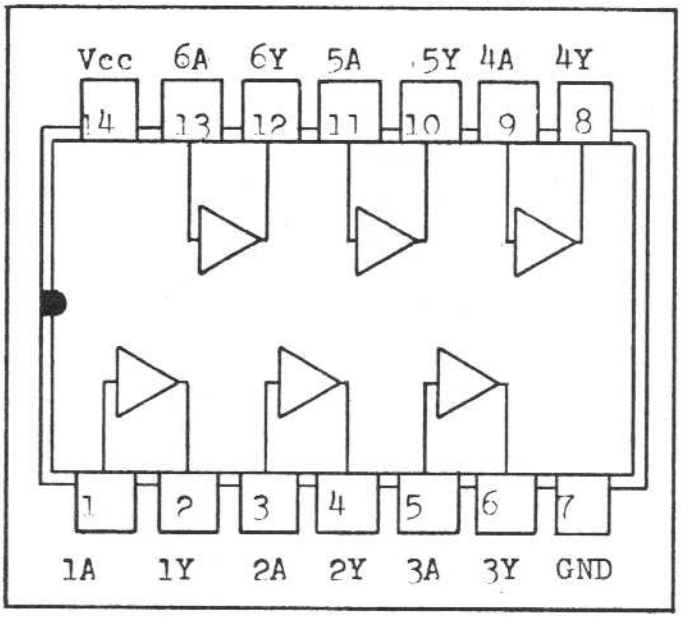
Switching Characteristics VCC-5V, TA-25 C

Parameter		Test Condition	MIN.	TYP.	MAX.	UNIT
TPLH	Propagation Delay Time, Low-To-High-Level Output	CL=15PF, RL=110 OHMS		17	26	NS
TPHL	Propagation Delay Time, High-To-Low Level Output	CL=15PF, RL=110 OHMS		10	15	NS

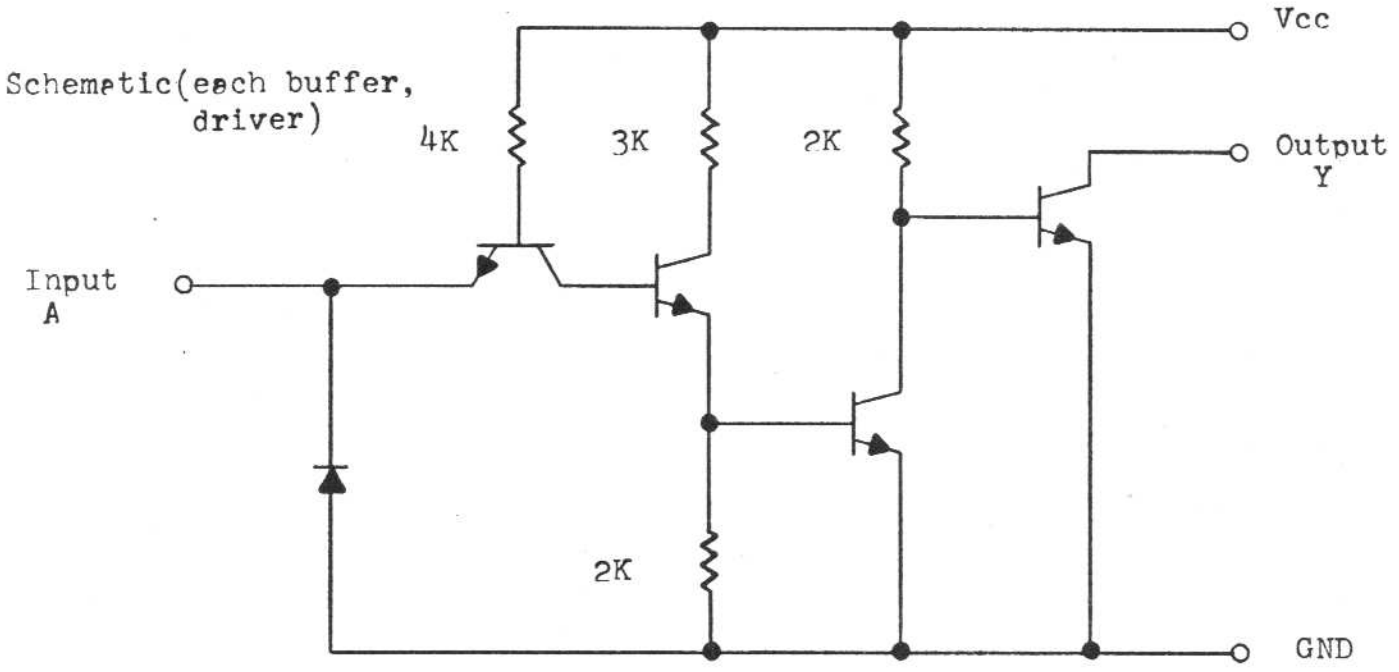
* NOTES: For conditions shown as max. or min., use the appropriate value specified under recommended operating conditions for the applicable device type.

** All Typical values are at VCC - 5V, TA - 25°C

PIN DIAGRAM (TOP VIEW)



Positive Logic: $Y = A$



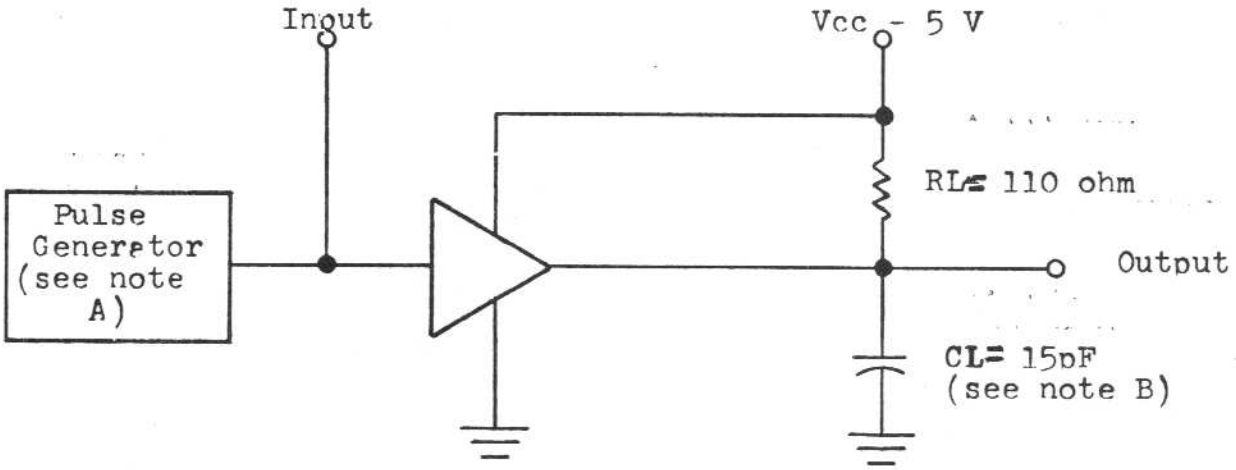
Note: Component values shown are norminal.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AC	B
SCALE:			SHEET 5 OF 6

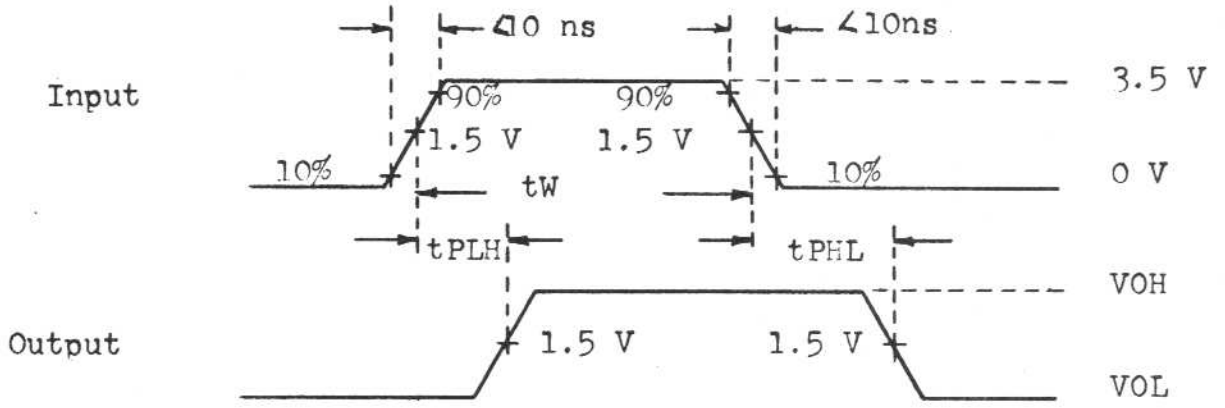
DO NOT SCALE PRINT

FORM A816-068-4/68

Switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

Notes:

A. The generator has the following characteristics: tW-0.5us, PRR-1MHz, Z-out-50 ohms

B. CL includes probe and jig capacitance

PROPAGATION DELAY TIMES

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AC	E
		SCALE:	SHEET 6 OF 6

DO NOT SCALE PRINT

FORM A816-058-4/68

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN # 4057		2/13/72	[illegible]

REV STATUS OF SHEETS	REV	A					A										
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
	DRAFTING		
	DESIGNED		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE

DUAL-IN-LINE PACKAGE I.C. SN74H78

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED		
LOCAL RELEASE		
CORPORATE RELEASE B. FRANKLIN	4 JUN 72	

SIZE		DRAWING NUMBER
A	B	C3313AD

DESIGNED FOR FOX-2

SCALE | WT | SHEET 1 OF 6

FORM 5758-C (5/69)

1.0 DESCRIPTION Dual-In-Line Package I. C. SN74H78 N

The J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections.

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line 14 Pin

3.0 PERFORMANCE CHARACTERISTICS

Supply Voltage: Min. 4.75 Volts
Nom. 5.0 Volts
Max. 5.25 Volts

Operating Free-Air Temp. Range: 0. to 70°C
Also see sheet # 3 and 4

4.0 QUALITY ASSURANCE PROVISIONS

Inspect per this drawing

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texas Instruments Incorporated
Dallas, Texas. P/N SN74H78-N-

OR EQUIVALENT FROM QUALIFIED VENDOR
WHO MEETS SPECIFICATIONS

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AD	A
		SCALE:	SHEET 2 OF 6

DO NOT SCALE PRINT

FORM A816-0SB-4/68

ELECTRICAL CHARACTERISTICS:(OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE UNLESS OTHERWISE NOTED)

PARAMETER:	** TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V-in(1) Input voltage required to ensure 1 at any input terminal	Vcc = Min.	2			Volts
V-in(0) Input voltage required to ensure 0 at any input terminal	Vcc= Min.			0.8	Volts
V-out(1) logical 1 output voltage.	Vcc=Min. Iload= 500 uA	2.4			Volts
V-out(0) logical 0 output voltage.	Vcc=Min. Isink=20 mA			0.4	Volts
I-in(0) level input current at J or K	Vcc=Max. V-in=0.4 V			-2	mA
I-in(0) level input current at preset or clock	Vcc= Max. V-in=0.4 V			-4	mA
I-in(0) level input current at clear	Vcc= Max. V-in=0.4 V			-8	mA
I-in(1) logical (1) level input current at J or K at clear.	Vcc=Max. V-in 2.4 V			50	uA
	Vcc=Max. V-in=5.5 V			1	mA
I-in(1) logical (1) level input current at preset or clock	Vcc=Max V-in=2.4 V			100	uA
	Vcc=Max. V-in=5.5 V			1	mA
I-in (1) logical (1) level input current at clear	Vcc=Max. V-in=2.4 V			200	uA
	Vcc=Max. V-in=5.5			1	mA
Ios Short-circuit output current	Vcc=Max. V-in=0. V	-40		-100	mA

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AD	A

DO NOT SCALE PRINT

SCALE:

SHEET 3 OF 6

FORM A816-088-4/68

ELECTRICAL CHARACTERISTICS CON'T

PARAMETER:	** TEST CONDITIONS:	MIN.	* TYP.	MAX.	UNIT:
Icc-Supply current	Vcc = Max.		32	50	mA

*-All typical values are at Vcc = 5 V, TA = 25°C
** For conditions shown as Min. or Max. use the appropriate value specified under recommended operating conditions for the applicable device type.

SWITCHING CHARACTERISTICS: Vcc = 5 Volts = 25°C N = 10

f clock Max. clock frequency	CL = 25pF RL = 280 ohms	25	30		MHz
** pdl Propagation delay time to logical 1 level from clear to output.	CL = 25pF RL = 280 ohms		6	13	ns
** pd(0) Propagation delay time to logical 0 level from clear to output.	CL = 25pF RL = 280 ohms		12	24	ns
** pd(1) Propagation delay time to logacal 1 level from clock to output.	CL = 25pF RL = 280 ohms		16	21	ns
** pd (0) Propagation delay time to logical 0 level from clock to output.	CL = 25pF 280 ohms		22	27	ns

** NOT MORE THAN ONE OUTPUT SHOULD BE SHORTED AT A TIME, AND DURATION OF SHORT-CIRCUIT TEST SHOULD NOT EXCEED 1 SECOND.

* FOR CONDITIONS SHOWN AS MAX. OR MIN, USE THE APPROPRIATE VALUE SPECIFIED UNDER RECOMMENDED OPERATING CONDITIONS FOR THE APPLICABLE DEVICE TYPE.

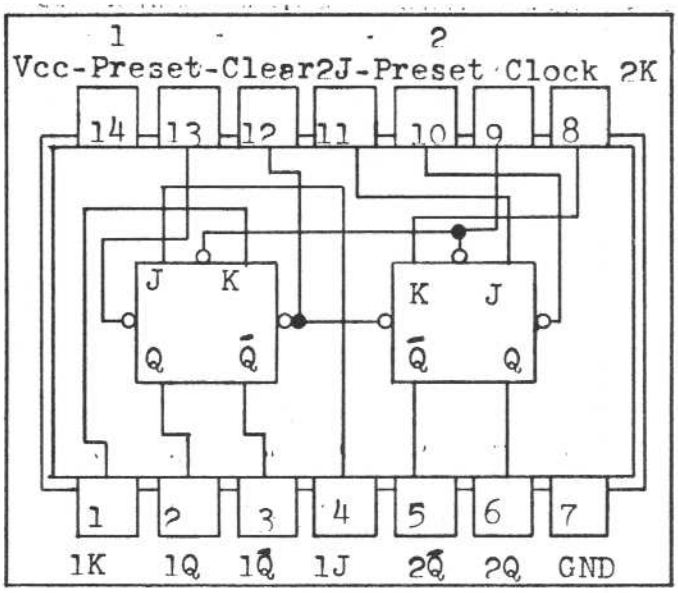
SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AD	A

DO NOT SCALE PRINT | SCALE: | SHEET 4 OF 6

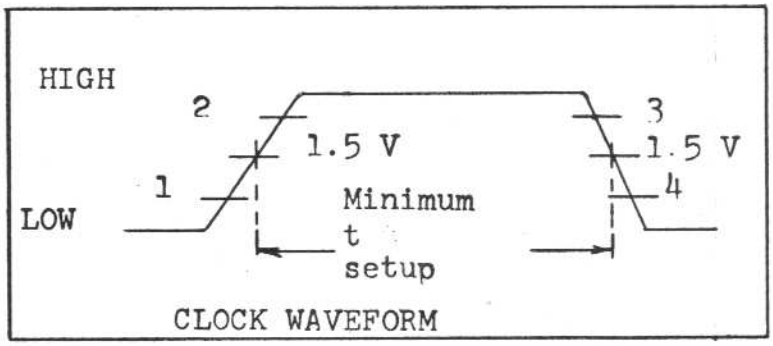
TRUTH TABLE		
tn		tn+1
J	K	Q
0	0	Qn
0	1	0
1	0	1
1	1	$\bar{Q}$n

NOTES: 1. tn- Bit time before clock pulse.

2. tn+1- Bit time after clock pulse.



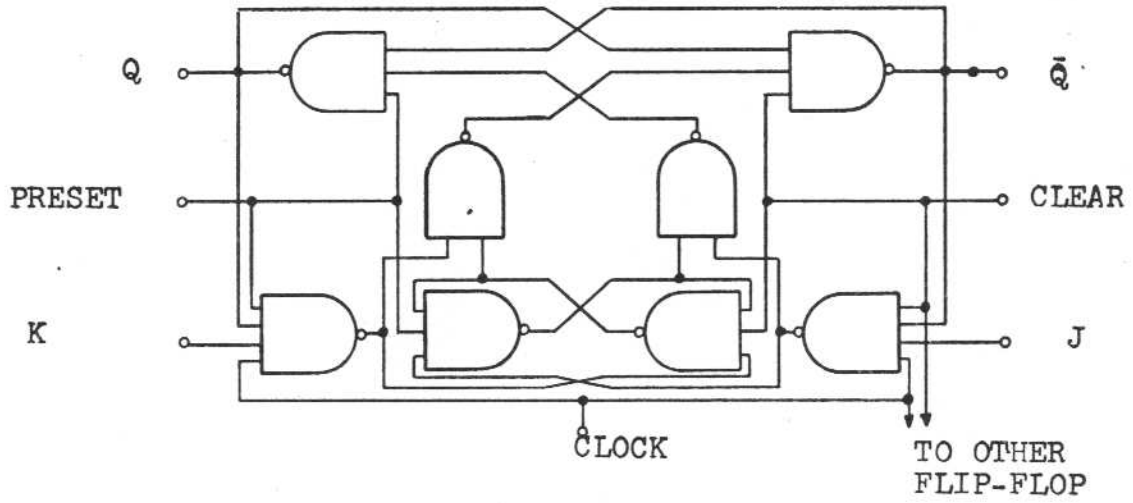
Positive Logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset and clear are independent of clock



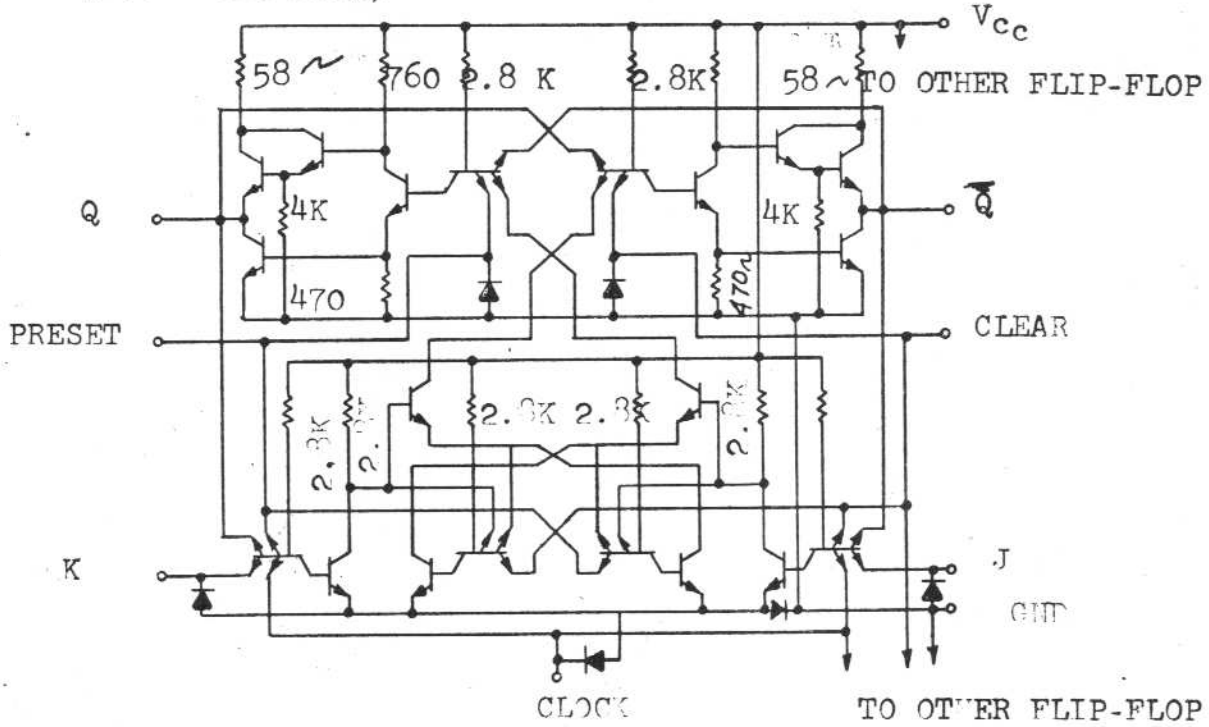
CLOCK WAVEFORM

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AD	A
DO NOT SCALE PRINT	SCALE:	SHEET 5 OF 6	

Functional block diagram (each flip-flop)



Schematic (each flip-flop)



SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AD	A
DO NOT SCALE PRINT	SCALE:	SHEET 6 OF 6	

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN # 4057 M		2/13/73	[illegible]

REV STATUS OF SHEETS																	
REV	A						A										
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
	DRAFTING		
	DESIGNED		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE

DUAL-IN-LINE PACKAGE I.C. SN7486

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED		
LOCAL RELEASE		
CORPORATE RELEASE B. FRANKLIN		14 JUNE

SIZE A B

DRAWING NUMBER C3313AE

DESIGNED FOR FOX-2

SCALE

WT

SHEET 1 OF 7

FORM 5758-C (5/69)

1.0 DESCRIPTION Dual-In-Line Package I.C. SN7486 N

Quadruple 2-input exclusive-or gates. Each of these monolithic, quadruple 2-input exclusive-OR gates utilize TTL circuitry to perform the function: $Y = A\bar{B} + \bar{A}B$. When the input states are complementary, the output goes to a logical 1.

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin

3.0 PERFORMANCE CHARACTERISTICS

Supply Voltage:	7 Volts
Input Voltage:(V in)	5.5 Volts (see note 1)
Operating free-air temp. Range:	0°C to 70°C
Storage Temp. Range:	- 65°C to 150°C

4.0 QUALITY ASSURANCE PROVISION

Inspect per this drawing.

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texas Instruments Incorporated
Dallas, Texas. P/N SN7486-N

Note: 1. These voltage values are with respect to network ground terminal.

OR EQUIVALENT FROM QUALIFIED VENDOR
WHO MEETS SPECIFICATIONS

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AE	A

DO NOT SCALE PRINT | SCALE: | SHEET 2 OF 7

Electrical Characteristics Con't

Recommended operating conditions (over operating temp. Range) SN7486

		Min.	Nom.	Max.	Unit.
Supply Voltage Vcc		4.75	5	5.25	Volts
Normalized fan-out each output N:	Logical 0			10.0	Volts
	Logical 1			20.0	Volts
Operating free-air temp. Range.		0		70.0	°C
V in (1)	Vcc = Min.	2.0			Volts
V in (0)	Vcc = Min.			0.8	Volts
V out (1)	Vcc = Min. V in (1) 2 V V in=(0) 0.8 V I load 800 uA	2.4			Volts
V out (0)	Vcc = Min. V in (1) 2 V V in=(0) 0.8 V			0.4	Volts
I in (1)	Vcc = Max. V in 2.4 V			40	uA
	Vcc = Max. V in 5.5 V			1	mA
I in (0)	Vcc = Max. V in 0.4 V			-1.6	mA
** IOS	Vcc = Max. 4.5 V Vin = (0) 0		-18	-55	mA
Icc	Vcc = Max. V in=4.5 V		30	50	mA

** Note: Not more than one output should be shorted at a time.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AE	A

DO NOT SCALE PRINT

SCALE:

SHEET 3 OF 7

FORM ABIE-088-4/68

Switching Characteristics: $V_{CC} = 5$ V $T_A = 25°$ C N 10

PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	Unit
tpd0	CL = 15 pF RL = 400 ohms		11	17	ns
tpd1	CL = 15 pF RL = 400 ohms		15	23	ns
tpd 0	CL = 15 pF RL = 400 ohms		13	22	ns
tpd 1	CL = 15 pF RL = 400 ohms		18	30	ns

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AE	A

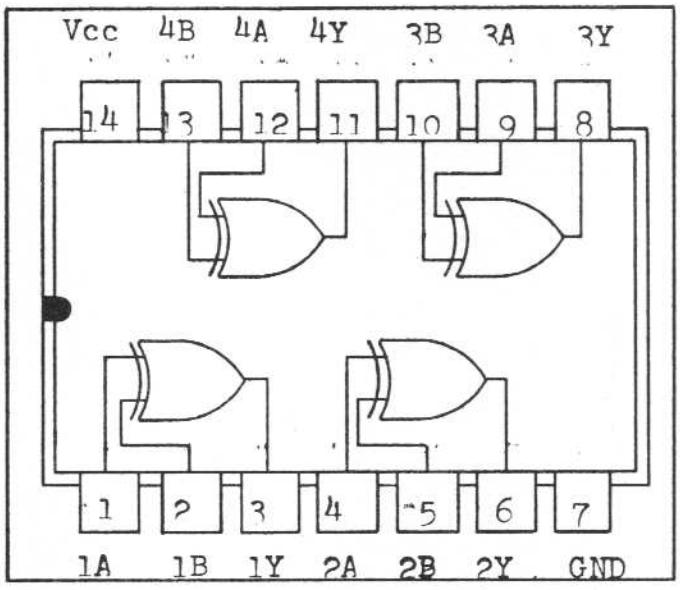
DO NOT SCALE PRINT

SCALE:

SHEET 4 OF 7

FORM A816-0SS-4/68

TRUTH TABLE		
Inputs		outputs
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



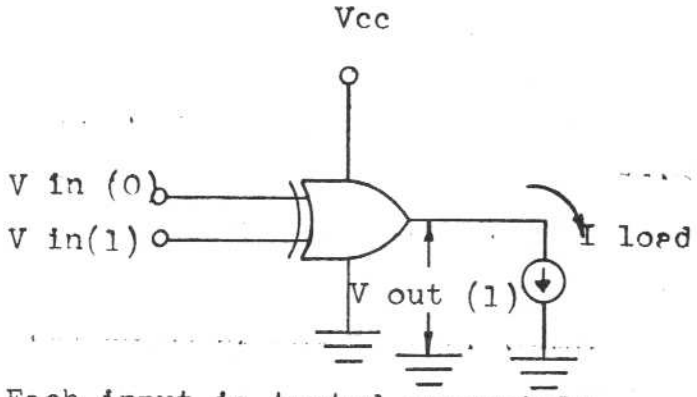
Positive Logic: Y=A ⊕ B

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AE	A
SCALE:			SHEET 5 OF 7

DO NOT SCALE PRINT

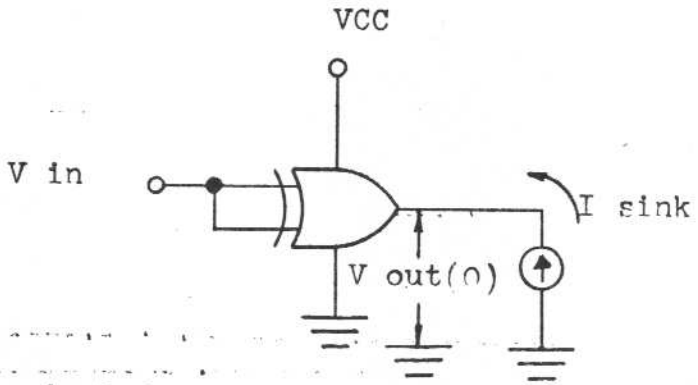
PARAMETER MEASUREMENT INFORMATION

d.c. test circuit



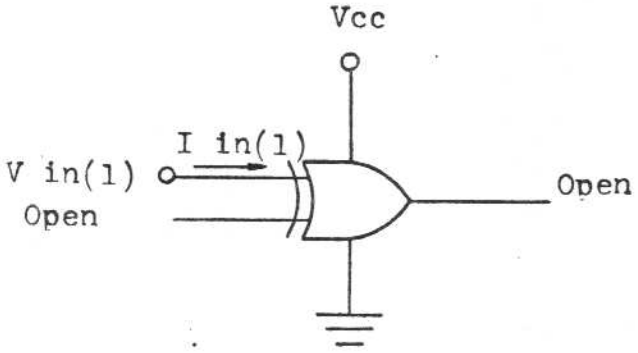
Each input is tested separately

Fig. 1



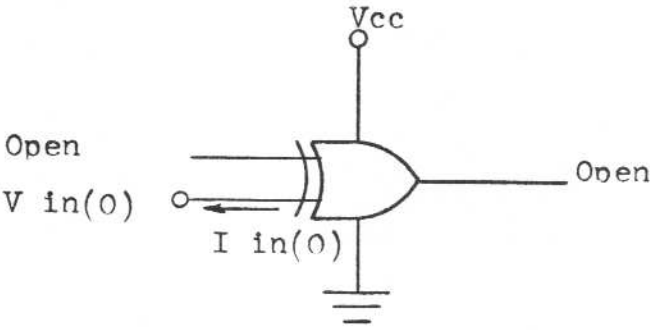
Logical 0 and logical 1 input conditions are tested

Fig. 2



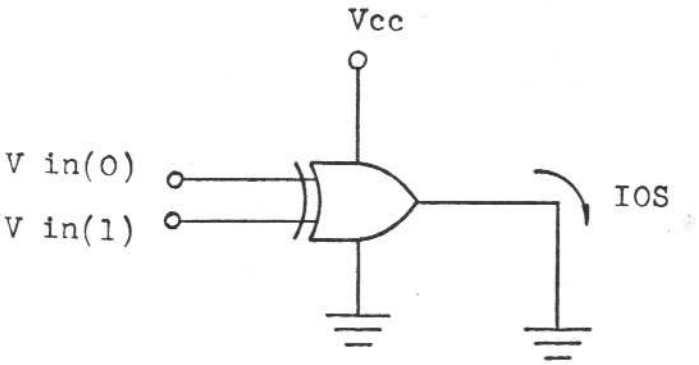
Each input is tested separately

Fig 3



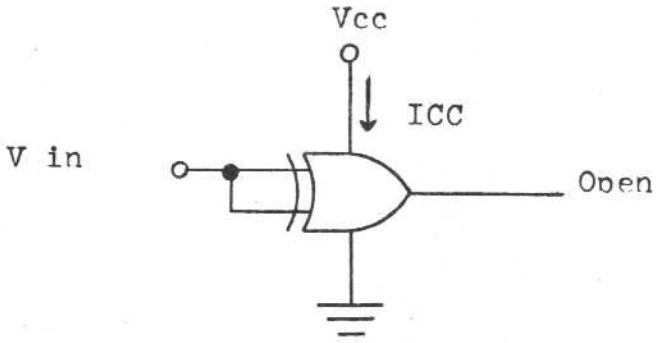
Each input is tested separately

Fig. 4



Each gate is tested separately

Fig 5



1. Each gate is tested separately
2. Logical 0 and logical 1 input conditions are tested

Fig 6

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AE	A

DO NOT SCALE PRINT

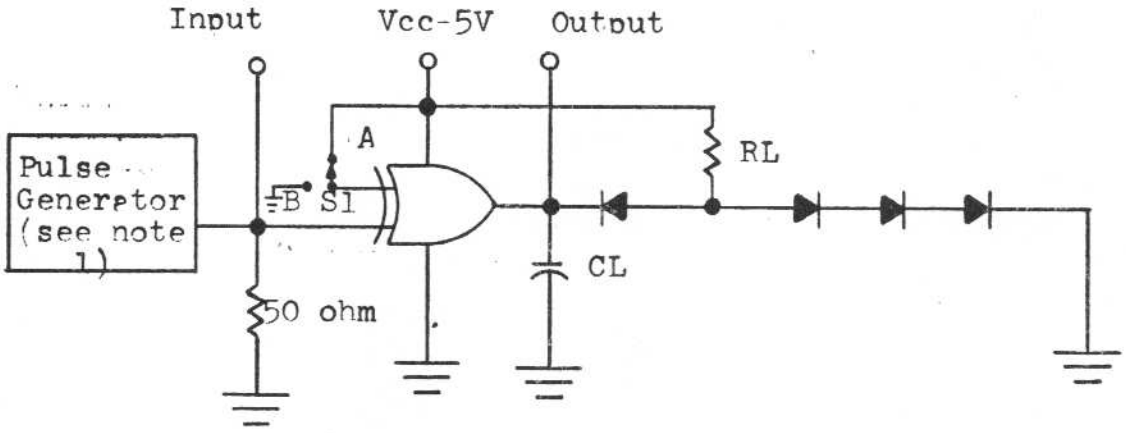
SCALE:

SHEET 6 OF 7

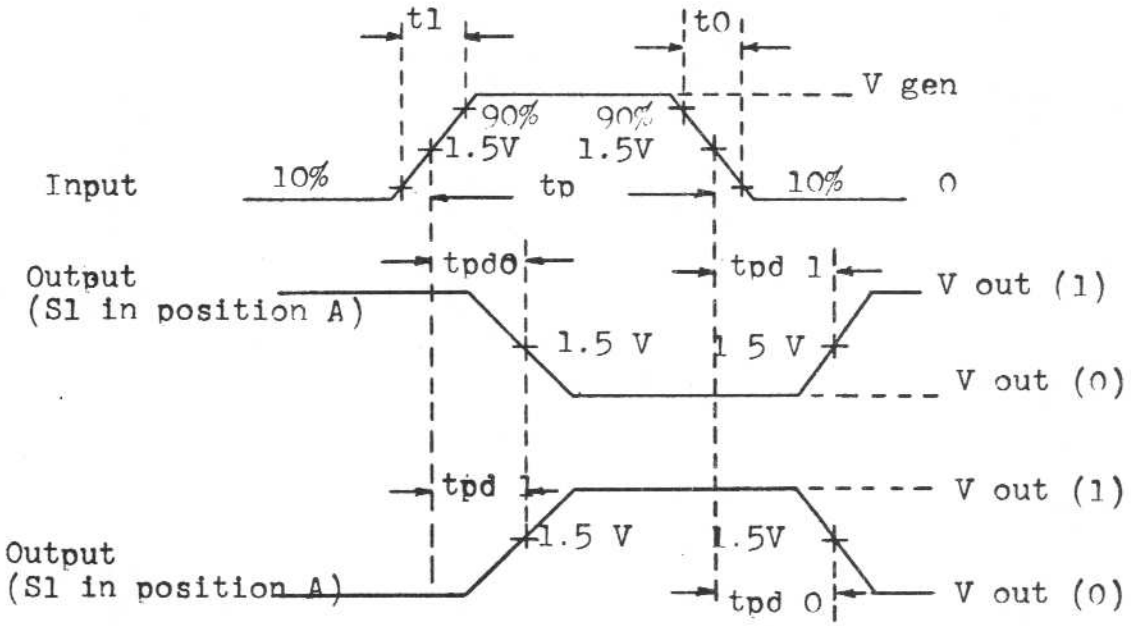
FORM ABIB-068-4/68

PARAMETER MEASUREMENT INFORMATION

Switching Characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:

1. The generator has the following characteristics
   V gen- 3 V`t o- t l≤15ns tp-0.5 us PRR-1MHz, Zout 50 ohm
2. All diodes are 1N3064
3. $tpd = \frac{tpd0 + tpd1}{2}$
4. CL includes probe and jig capacitance
5. Each gate tested separately

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AE	A

DO NOT SCALE PRINT | SCALE: | SHEET 7 OF 7

FORM A816-088-4/68

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN # 4057		2/13/72	M/Cook

REV STATUS OF SHEETS																	
REV	A				A												
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
	DRAFTING		
	DESIGNED		8/17/71
	APPROVED		
	LOCAL RELEASE		
	CORPORATE RELEASE	B. FRANKLIN	14 JUN 72

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE

DUAL-IN-LINE PACKAGE SN74164

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

DESIGNED FOR Fox-2

SIZE		DRAWING NUMBER
A	B	C3313AF

SCALE	WT	SHEET 1 OF 5

FORM 5758-C (5/69)

1.0 DESCRIPTION

8-Bit Parallel-Out Serial Shift Registers.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin

3.0 PERFORMANCE CHARACTERISTICS

Supply Voltage: 5 Volts
Low-Level (Logical 0) Output Voltage: 0.2 Volts
High-Level (Logical 1) Output Voltage: 3.3 Volts
Noise Immunity: 1 Volt
Storage Temp. Range: 0°C to 70°C
Power Dissipation Typical: 180 Milliwatts
Maximum Input Clock frequency typical: 20 Megahertz

4.0 QUALITY ASSURANCE PROVISIONS

Inspect per this drawing.

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texas Instruments
Dallas, Texas P/N SN74164

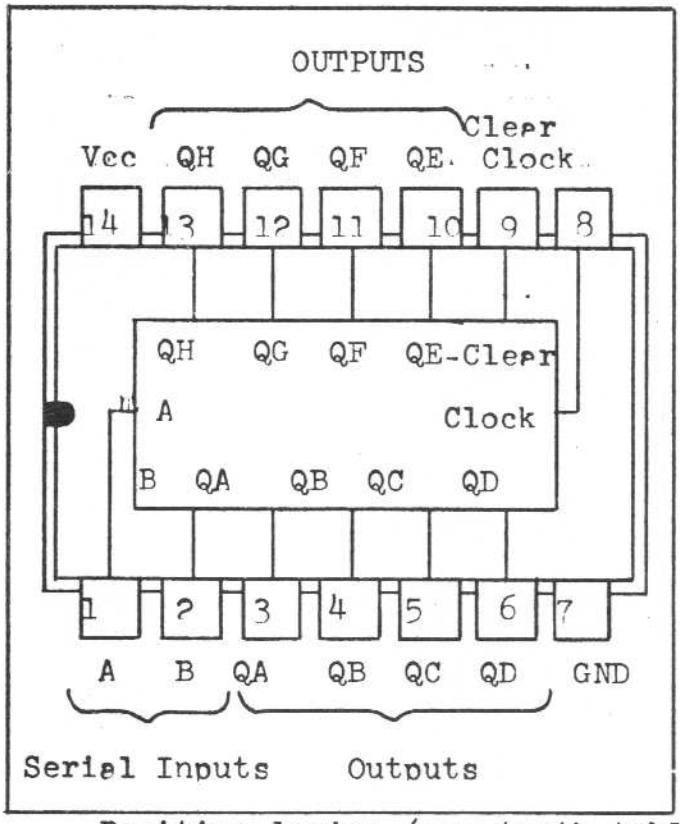
OR EQUIVALENT FROM QUALIFIED VENDOR
WHO MEETS SPECIFICATIONS

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AF	4
		SCALE:	SHEET 2 OF 5

DO NOT SCALE PRINT

SERIAL INPUTS A & B

TRUTH TABLE		
Inputs(tn)		Output(tn-1)
A	B	QA
H	H	H
L	H	L
H	L	L
L	L	H



Positive logic; (see truth table)

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AF	A
SCALE:		SHEET 2 OF 5	

DO NOT SCALE PRINT

FORM A816-0888-4/88

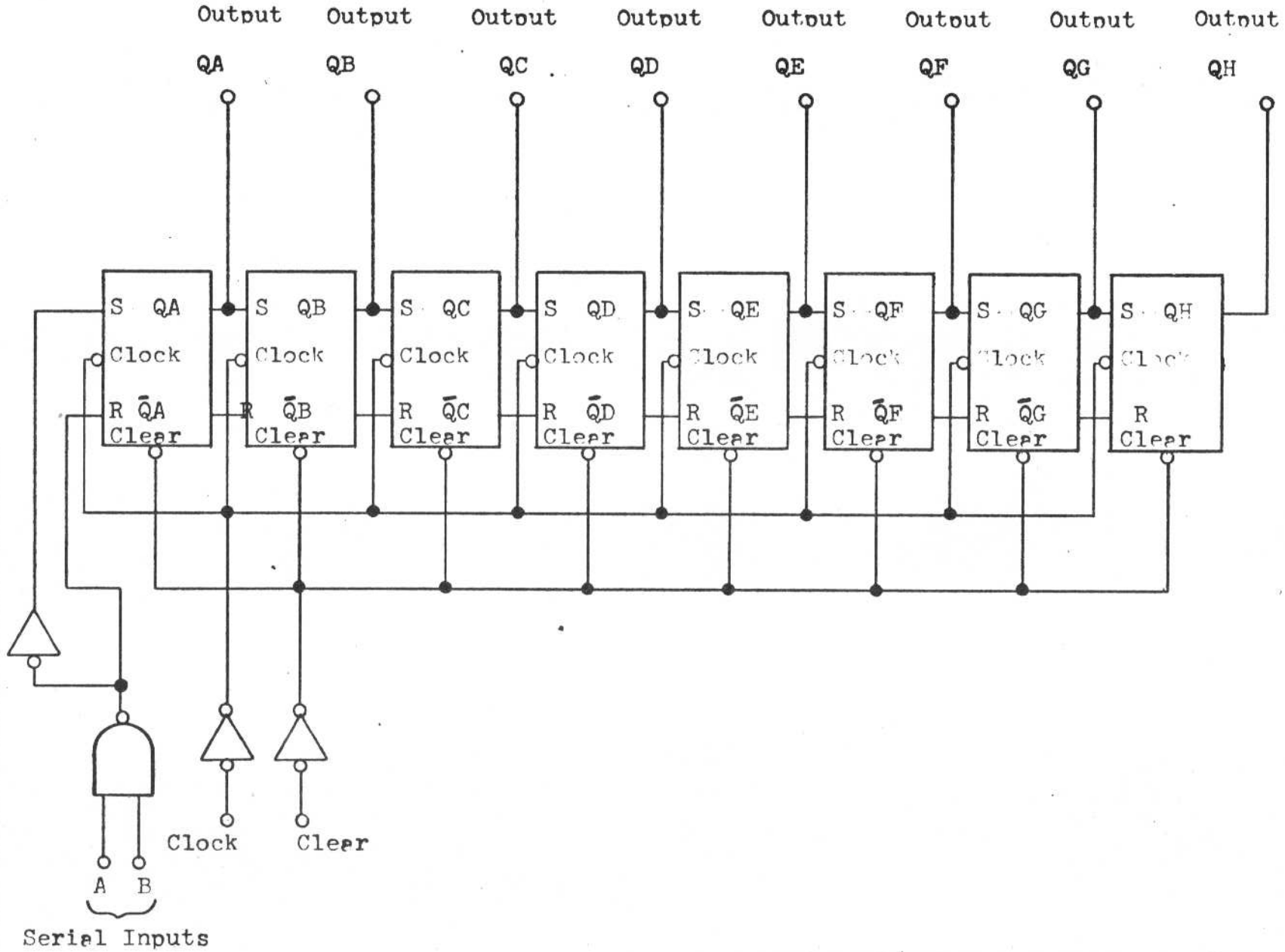
DO NOT SCALE PRINT

SIZE A B | SYMBOL | DRAWING NO. 82218AB | REV 4

SCALE:

SHEET 4 OF 5

Functional block diagram



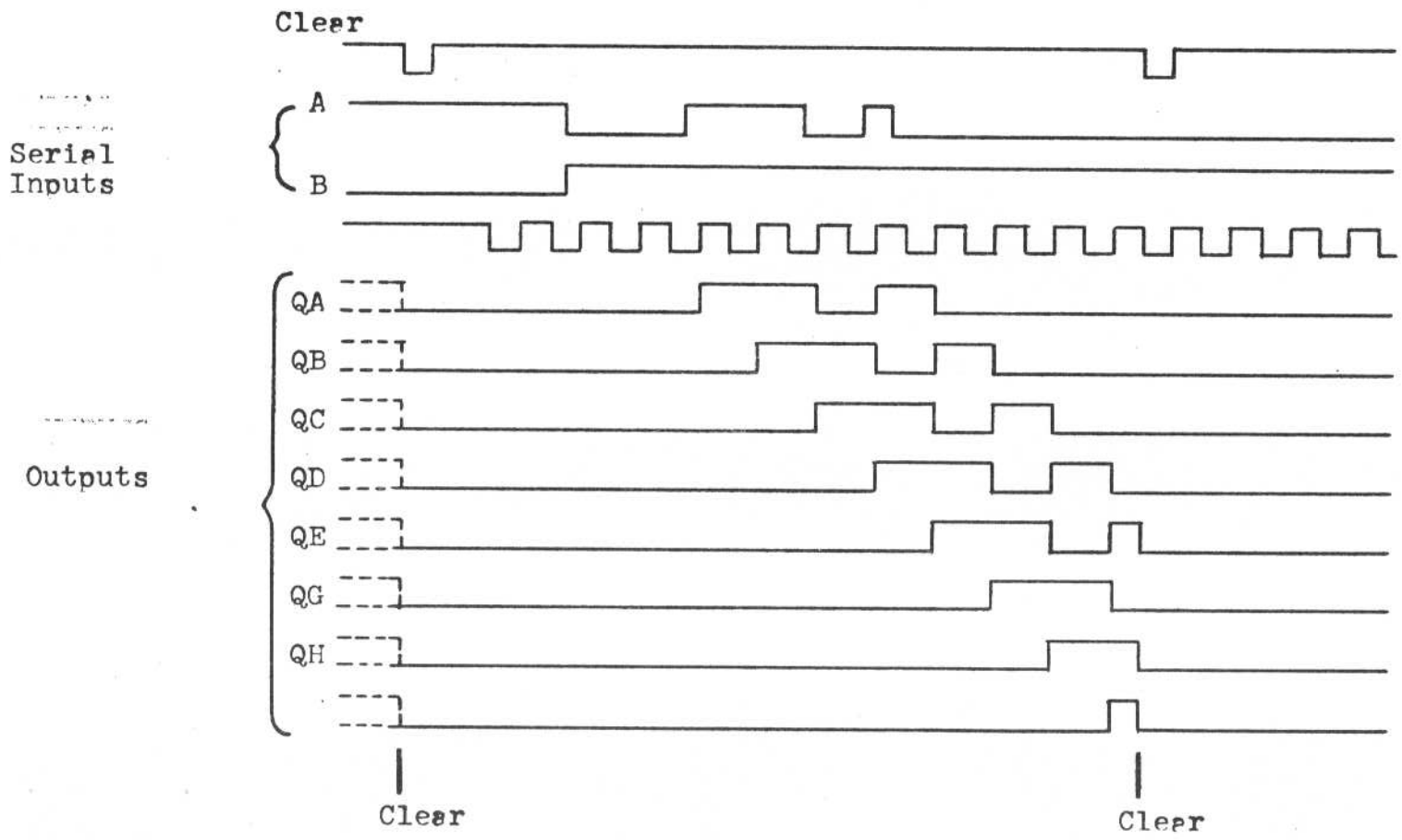
DO NOT SCALE PRINT

FORM A816-0088-4/88

SIZE A | SYMBOL B | DRAWING NO. C3212AF | REV

SCALE: | SHEET 5 OF 5

Typical clear, inhibit, shift, clear, and inhibit sequences



REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	Local Release Per ECN # M			

REV STATUS OF SHEETS	REV																
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
	DRAFTING		
	DESIGNED		
	checked Nelson	6/72	
	APPROVED		
	LOCAL RELEASE		
	CORPORATE RELEASE		

SUPERSEDING
INTERCHANGEABLE YES
SIMILAR TO NO

DESIGNED FOR

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE

DUAL-IN-LINE PACKAGE I.C. SN7406

SIZE		DRAWING NUMBER
A	B	C3313AG

SCALE	WT	SHEET 1 OF 17

FORM 5758-C (5/69)

1.0 DESCRIPTION Dual-In-Line Package I. C. SN7406 N

Hex Inverter, Buffers/drivers with open collector high voltage outputs. For interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays)and are also characterized for use as inverter buffers for driving TTL inputs.

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin

3.0 PERFORMANCE CHARACTERISTICS

Supply Voltage:	7 Volts (See note 1)
Input Voltage:	5.5 Volts (See note 1)
Output Voltage:	30 Volts (See note 1 and 2
Operating free-air temp. range:	- 55°C to 125°C
Storage Temp. range:	-65°C to 150°C

Also see sheet # 3 and # 4

4.0 QUALITY ASSURANCE PROVISION

Inspect per this drawing.

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texas Instruments Incorporated
Dallas, Texas. P/N SN7406-N

Notes:
1. Voltage values are with respect to network ground terminal.
2. This is the Max. voltage which should be applied to any output when it is in the off state.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AG	A
		SCALE:	SHEET 2 OF 7

DO NOT SCALE PRINT

FORM A816-088-4/66

Electrical Characteristics: Cont't

Recommended Operating Conditions

	SN7406			
	MIN.	NOM.	MAX.	UNIT
Supply Voltage Vcc	4.75	5	5.25	Volts
Output Voltage VOH			30	Volts
Low-level output Current, IOL			40	mA
Operating free-air temperature range, TA	0	25	70	°C

PARAMETER	TEST CONDITIONS *	MIN.	TYP.	MAX.	UNIT
VIH		2			Volts
VIL				0.8	Volts
IOH	Vcc = Min. Vl 0.8 V. VOH = Max.			250	uA
VOL	Vcc = Min. Vl 2 V IOL = Max. 16 mA			0.7 0.4	Volts Volts
IIH	Vcc = Max. Vl 2.4 V Vcc = Max. Vl 5.5 V			40 1	uA mA
IIL	Vcc = Max. Vl 0.4 V			-1.6	mA
IccH	Vcc = Max. Vl 0		30	42	mA
IccL	Vcc = Max. Vl 5 V		27	38	mA

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

* For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at Vcc 5 V TA 25°C

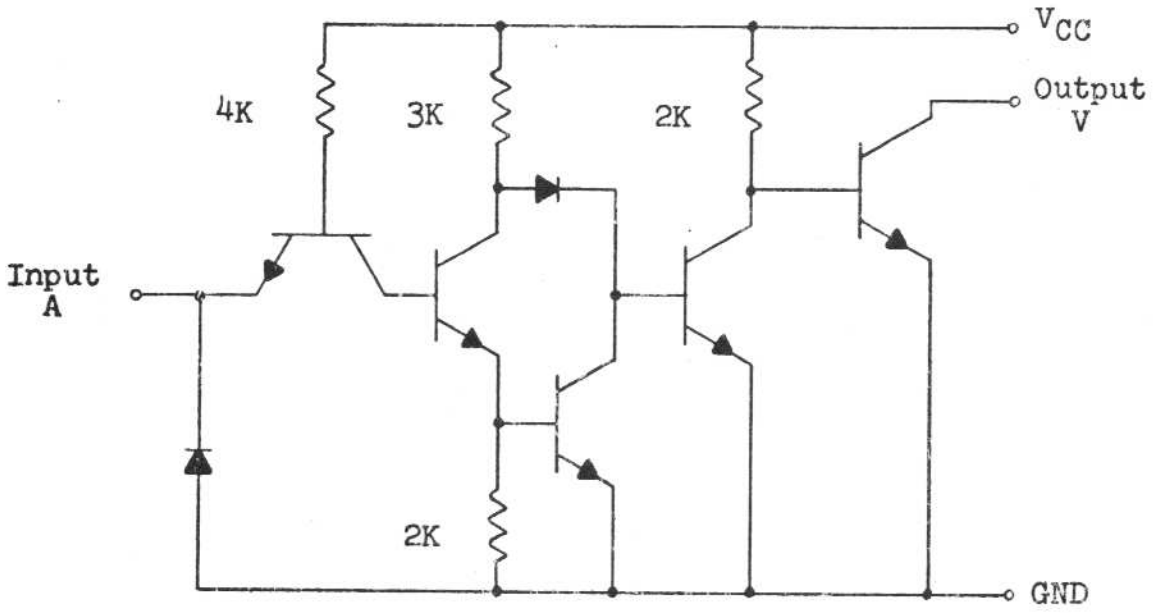
Switching Characteristics, Vcc 5 V TA 25°C

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
tPLH	CL = 15pF RL = 110 Ohms		17	26	ns
tPHL	CL = 15pF RL = 110 Ohms		13	20	ns

SIZE	SYMBOL	DRAWING NO.	REV
A		C3713AG	A
	SCALE:		SHEET 4 OF 17

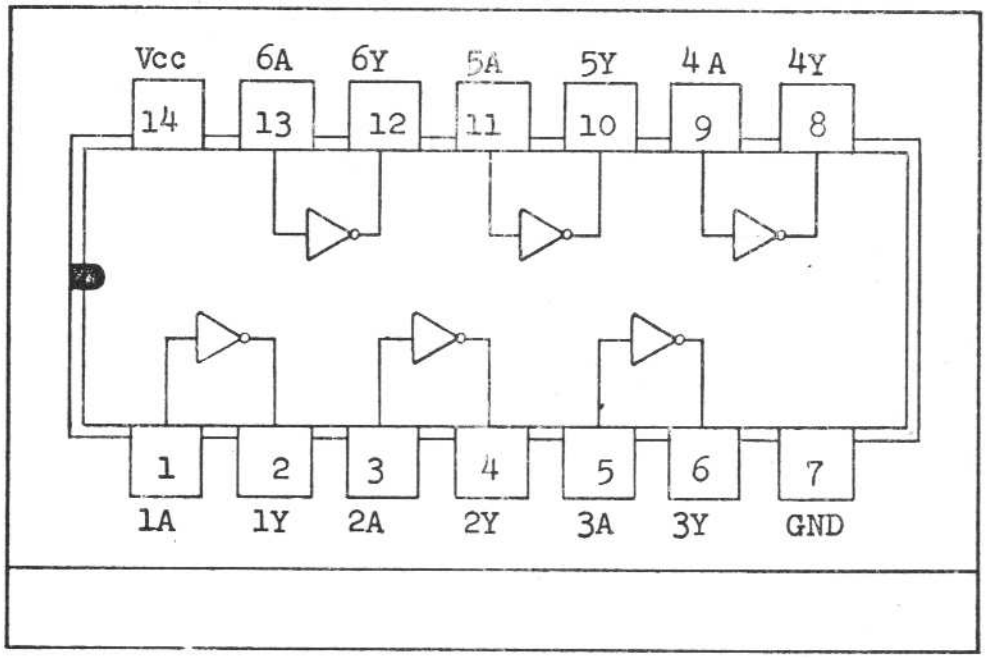
DO NOT SCALE PRINT

Schematic (Each Inverter)



NOTE: Component values shown are nominal.

J or N
Dual-In-Line Package
(Top View)



SIZE	SYMBOL	DRAWING NO.	REV
A		C3313AG	A
		SCALE:	SHEET 5 OF 7

DO NOT SCALE PRINT

PARAMETER MEASUREMENT INFORMATION

d-c test circuits

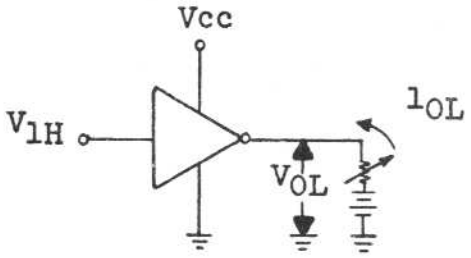


FIGURE 1 - V_{1H} V_{OL}

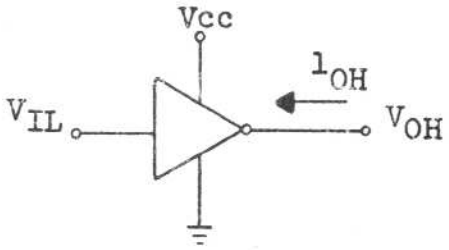


FIGURE 2 - V_{1L} I_{OH}

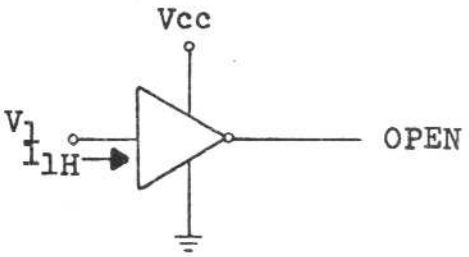


FIGURE 3 - I_{1H}

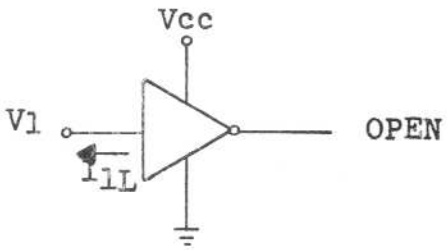
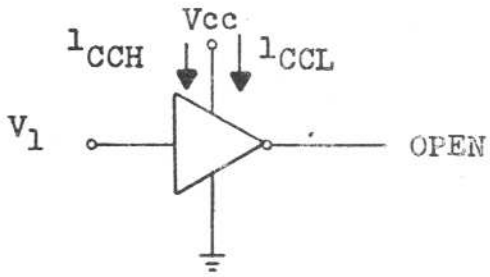


FIGURE 4 - I_{1L}



All inverters are tested simultaneously.

FIGURE 5 - I_{CCH} I_{CCL}

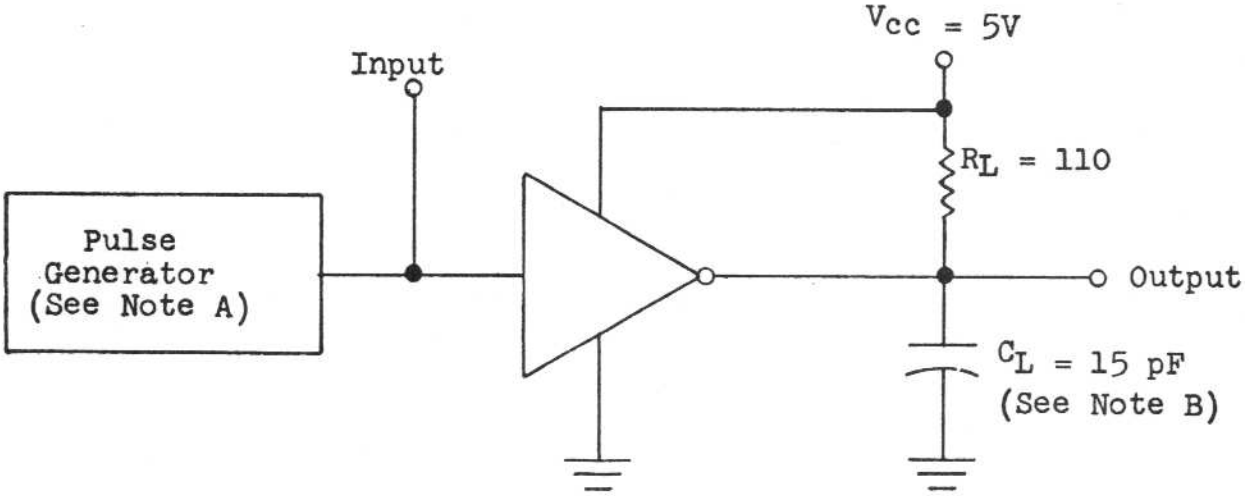
Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

SIZE	SYMBOL	DRAWING NO.	REV
A	15	C3313AG	A
	SCALE:		SHEET 6 OF 7

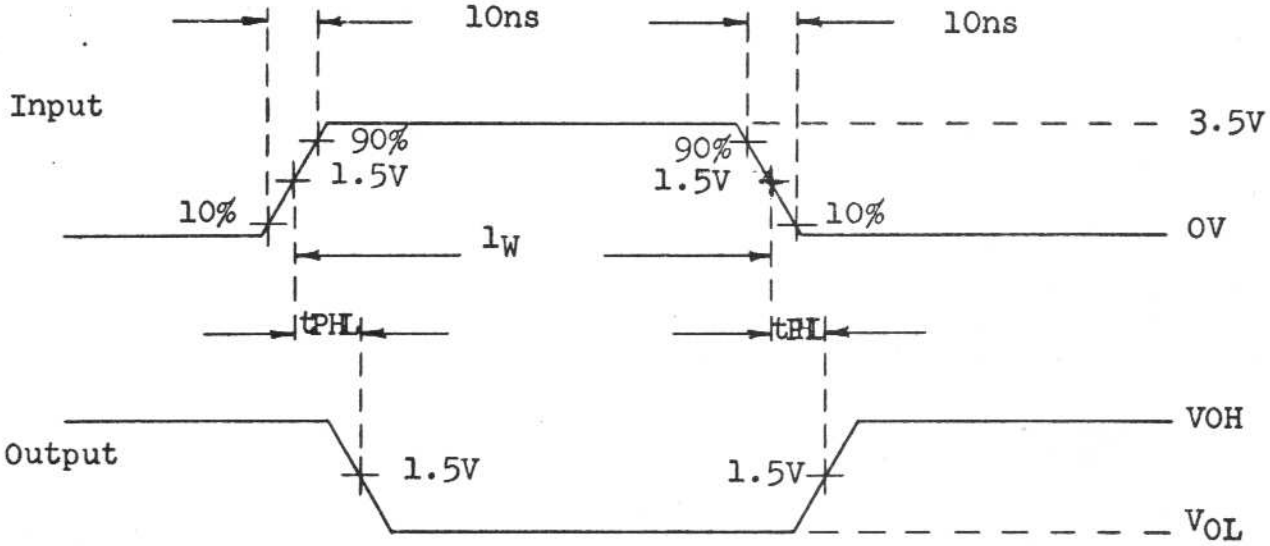
DO NOT SCALE PRINT

PARAMETER MEASUREMENT INFORMATION

Switching Characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: tW=0.5 us, PRR=1 MHz, Zout = 50
B. C_L includes probe and jig capacitance.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AG	A
DO NOT SCALE PRINT	SCALE:	SHEET 7 OF 7	

FORM ABIB-088-4/68

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	M LOCAL RELEASE PER ECN # 4080		3/13/72	MJC

REV STATUS OF SHEETS	REV	A	←				→	A									
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

DRAWN	CHK'D M. Kelly	DATE 4Nov71
DRAFTING		
DESIGNED E. Hoffer		9/20/71
APPROVED		9/20/71
LOCAL RELEASE MJC		
CORPORATE RELEASE		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE

DUAL-IN-LINE PACKAGE I.C. SN7417N

SUPERSEDING
INTERCHANGEABLE YES / NO
SIMILAR TO

DESIGNED FOR FOX-2

SIZE		DRAWING NUMBER
A	B	C3313AH

SCALE NONE | WT | SHEET 1 OF 7

FORM 5758-C (5/69)

1.0 DESCRIPTION Dual-In-Line Package I.C. SN7417N Plastic-Pkg.

These monolithic TTL hex buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high current loads. (such as lamps or relays), and are also characterized for use as buffers for driving TTL inputs.

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin
Vendor P/N marked on case.

3.0 PERFORMANCE CHARACTERISTICS

See tables #1. 2. 3.

Notes:

(1) Voltage values are respect to network ground terminal.

(2) This is the maximum voltage which should be applied to any output when it is the off state.

4.0 QUALITY ASSURANCE PROVISIONS

Inspect per this drawing

5.0 MANUFACTURER'S NAME AND PART NUMBER

Texas Instruments, Incorporated
Dallas, Texas.
P/N # SN7417

Table # 1

Recommended operating conditions

	Min.	Nom.	Max.	Unit
Supply Voltage VCC:	4.75	5	5.25	Volts
Output Voltage VOH:			15	Volts
Low-Level output current, IOL :			40	mA
Operating free-air temp. Range:	0	25	70	°C

Table # 2

Electrical characteristics over recommended operating free-air Temp. Range:

Parameter	test condition	Min.	Typ	Max.	Unit.
VIH High-level input voltage:		2			Volts
VIL Low-level input voltage:				0.8	Volts
IOH High-level output current:	VCC=Min. Vl= 2V VOH=Max.			250	uA
VOL Low-level output voltage	Vcc=Min Vl=0.8 V IOL=Max.			0.7	Volts
	VCC-Min. Vl=0.8 V IOL-Max.			0.4	Volts
IIH High-level input current (each input)	VCC=Max. Vl-2.4 V			40	uA
	VCC-Max. Vl=5.5			1	mA

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AH	A
DO NOT SCALE PRINT	SCALE: NONE	SHEET 3 OF 7	

Electrical Characteristics Table #2 Cont

Parameter	test condition	Min.	Typ.	Max.	Unit
IIL Low-level input current (each input)	Vcc-Max. Vl-0.4 V			-1.6	mA
ICCH Supply current high-level output	Vcc-Max. Vl-5 V		29	41	mA
ICCL Supply current low-level output	Vcc-Max. Vl-0		21	30	mA

Switching Characteristics, Vcc-5V TA-25°C

Table #3

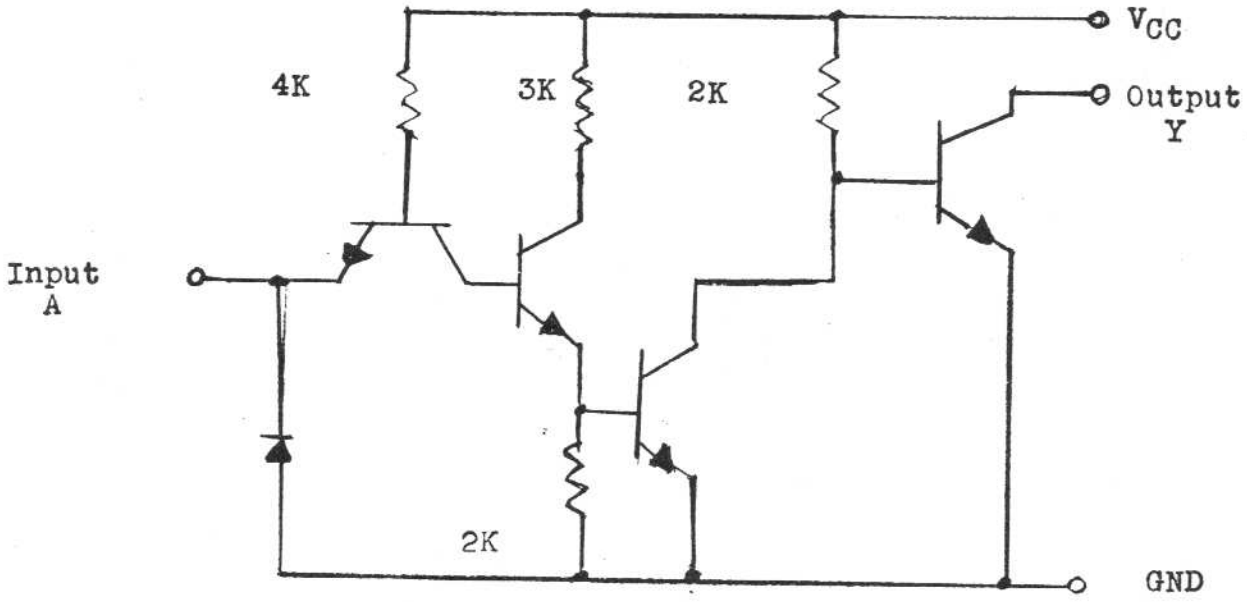
Parameter	test condition	Min.	Typ.	Max.	Unit.
tPLH Propagation delay time, low-to-high-level output	C_L = 15pF, R_L = 110 Ohm		17	26	ns
tPHL Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 110 Ohm		10	15	ns

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AH	A
		SCALE: NONE	SHEET 4 OF 7

DO NOT SCALE PRINT

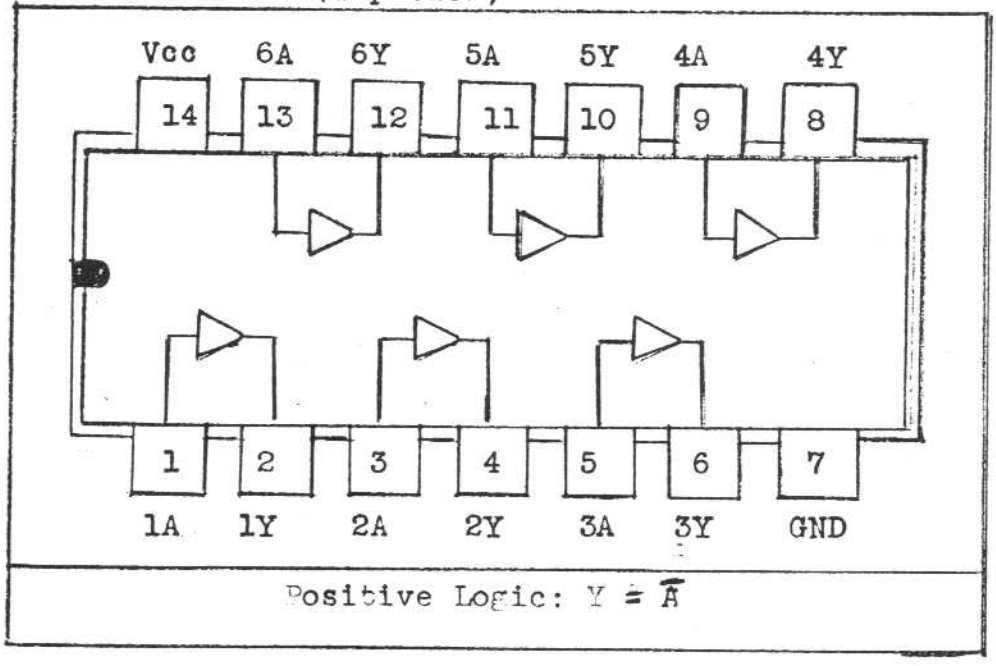
FORM A816-068-4/68

Schematic (Each buffer/driver)



NOTE: Component values shown are norminal.

J or N
Dual-In-Line Package
(Top View)



Positive Logic: $Y = \overline{A}$

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C331 3AH	A
SCALE: NONE		SHEET 5 OF 7	

DO NOT SCALE PRINT

PARAMETER MEASUREMENT INFORMATION

d-c test circuit

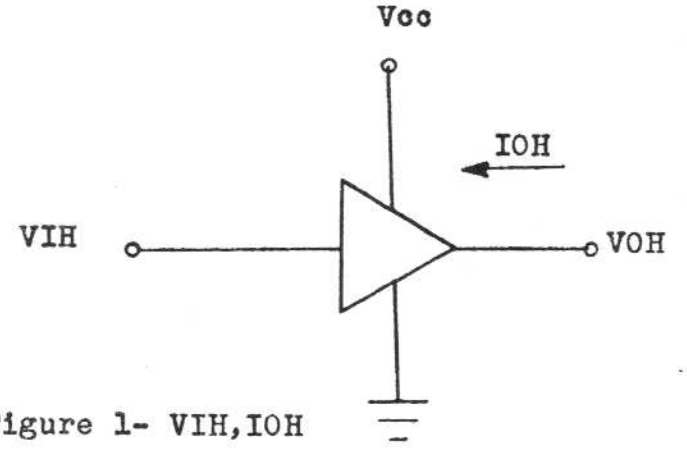


Figure 1- VIH,IOH

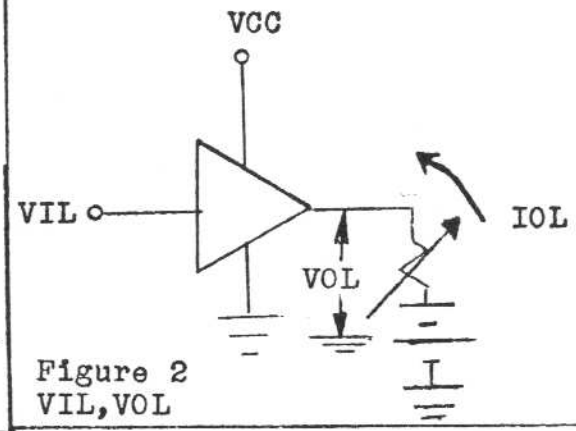


Figure 2
VIL,VOL

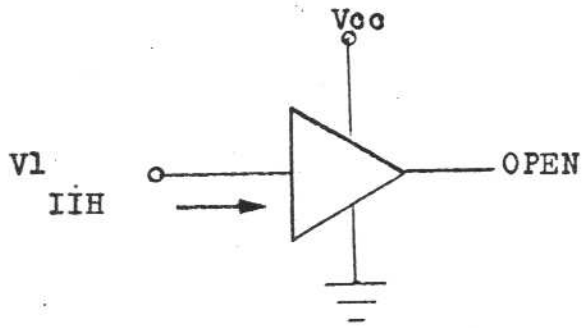


Figure 3-IIH

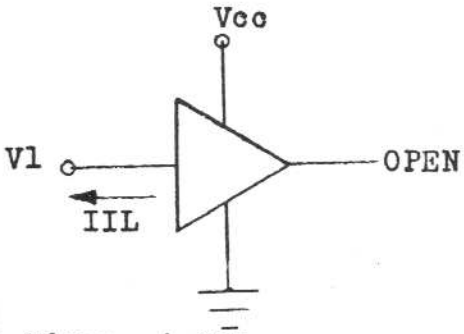
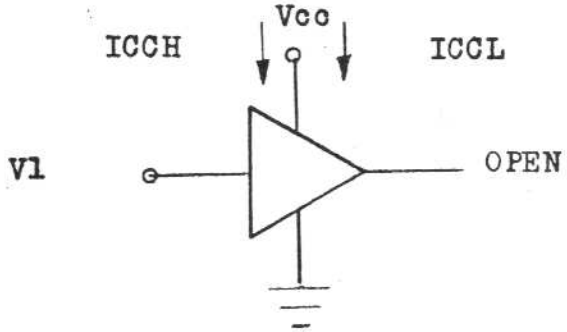


Figure 4-IIL



All buffers/drivers are tested simultaneously.

FIGURE 5- I CCH I CCL

Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

SIZE	SYMBOL	DRAWING NO.	REV
A	D	C3313AH	A

DO NOT SCALE PRINT

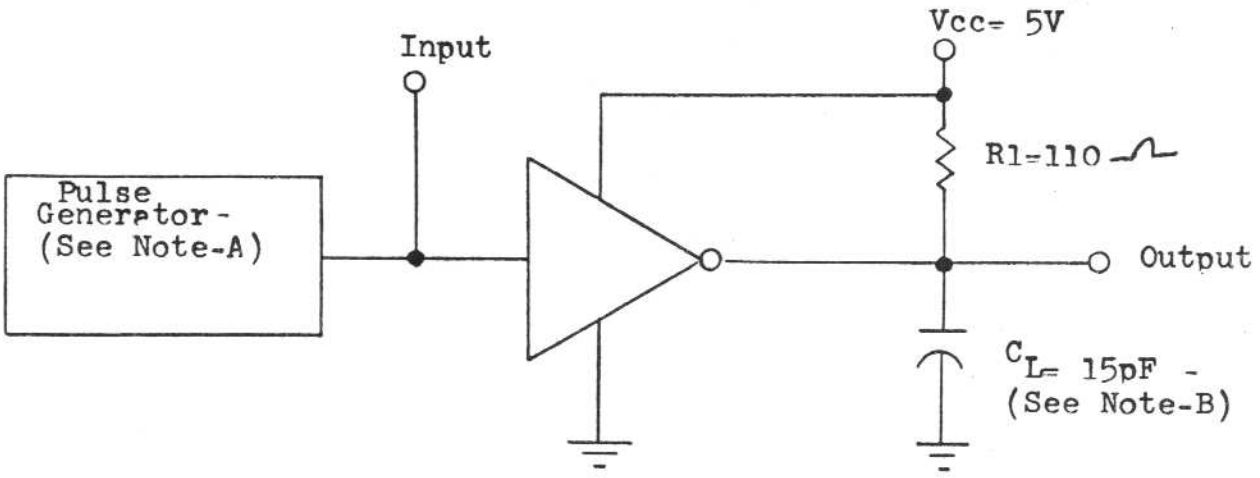
SCALE: NONE

SHEET 6 OF 7

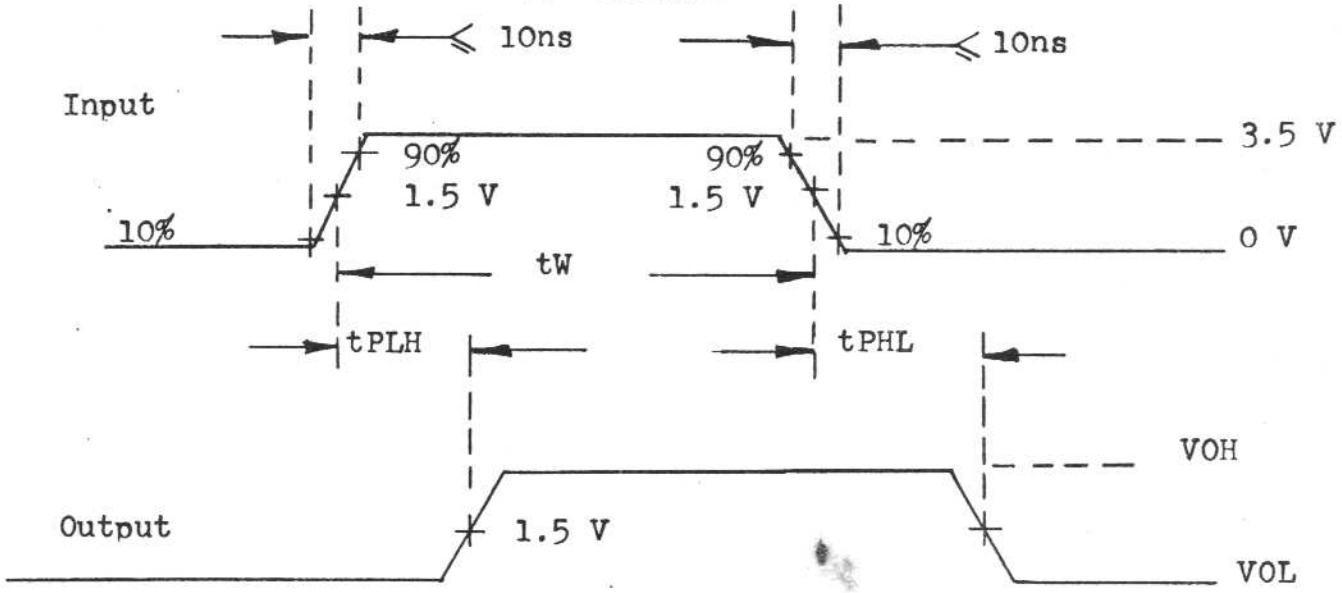
FORM A816-088-4/68

PARAMETER MEASUREMENT INFORMATION

Switching Characteristics



Test Circuit



Voltage Waveforms

Notes: (A) The generator has the following characteristics: tW= 0.5 us, PRR= 1 MHZ, Z out≈50Ω

(B) CL includes probe and jig capacitance.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AH	A
		SCALE: None	SHEET 7 OF 7

DO NOT SCALE PRINT

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN # 4057		2/13/72	[illegible]

REV STATUS OF SHEETS	REV	A	A	A													
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
	DRAFTING		
	DESIGNED		2/2/72
	APPROVED		
	LOCAL RELEASE		2/14/72
DESIGNED FOR Fox-2	CORPORATE RELEASE B. FRANKLIN		6/29/72

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE

DUAL-IN-LINE PACKAGE SN7437

SUPERSEDING INTERCHANGEABLE SIMILAR TO YES NO

SIZE		DRAWING NUMBER
A	B	C3313AJ
SCALE	WT	SHEET 1 OF 3

FORM 5758-C (5/69)

1.0 DESCRIPTION

Quadruple 2-Input Positive NAND Buffers SN7437

The NAND gate buffers feature very high fan-out capabilities (N-30).

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14-Pin

3.0 PERFORMANCE CHARACTERISTICS

Supply Voltage: 5 Volts
Low Level (Logical 0) Output Voltage: 0.2 Volts
High-Level (Logical 1) Output Voltage: 3.3 Volts
Noise Immunity: 1 Volt
Storage Temp. Range: 0°C to 70°C

4.0 QUALITY ASSURANCE PROVISIONS

Inspect per this drawing.

5.0 MANUFACTURER'S NAME AND PART NUMBER

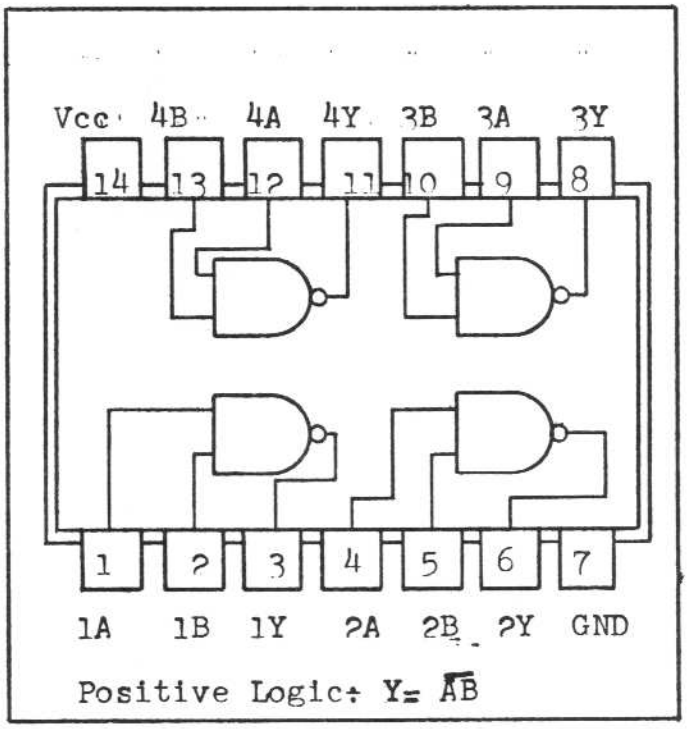
Texas Instruments, Inc.
Dallas, Texas P/N SN7437

OR EQUIVALENT FROM QUALIFIED VENDOR
WHO MEETS SPECIFICATIONS

SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AJ	A
		SCALE:	SHEET 2 OF

DO NOT SCALE PRINT

FORM A816-088-4/66



SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AJ	A
SCALE:		SHEET 3 OF 3	

DO NOT SCALE PRINT

FORM A818-088-4/68

REVISIONS				
	DESCRIPTION	CODE	DATE	REVIEWED BY APPROVED BY

FAB SEPIA CHANGE

F.S.C. # 1A-1

S.D. CODE —

INDICATOR 12

ENGINEER [illegible]

DATE 5 DEC 72

REV STATUS OF SHEETS	REV	1A-1	1A-1	1A-1	1A-1	1A											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED DECIMAL DIMENSIONS ± .020 ANGLES ± 1°	DRAWN	CHK'D	DATE
	DRAFTING		
	DESIGNED		
	APPROVED		
	ENGR RELEASE		
	CUSTOMER RELEASE		

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE

~~THIS SCHEM. DIAG.~~

QUAD-2 INPUT OR GATE

F.S.C. #1A-1

INTERCHANGEABLE	YES / NO	SIZE	DRAWING NUMBER
SUPERSEDES			C8313AL
SUPERSEDED BY		SCALE	WT / SHEET 1 OF 2

FORM 5758-C (5-69)

1.0 DESCRIPTION Quad-2-Input, POSITIVE OR GATE F.S.C. # 1A-1.

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14 Pin; FOR PIN ASSIGNMENTS F.S.C. # 1A-1

See Fig. 1

3.0 PERFORMANCE CHARACTERISTICS

(Absolute Maximum Rating) See Notes 1, 2, 3, and 4

Voltage Applied: (All Terminals) ±5.5 V F.S.C. # 1A-1

~~Current Rating. (All Input Terminals) 5 Ter~~ F.S.C. # 1A-1

~~(All Output Terminals)~~

Temp. Operating Range: 0°C to + 75°C
Temp. Storage Range: - 65°C to - 150°C

4.0 QUALITY ASSURANCE PROVISIONS

Inspect per this drawing

5.0 MANUFACTURER'S NAME AND PART NUMBER

SIGNETICS, Corporation
811 East Arques Avenue
Sunnyvale, California. (A Subsidiary of Corning Glass Works)

P/N # SP334A

SIZE	SYMBOL	DRAWING NO.	REV
A			
DO NOT SCALE PRINT	SCALE:	SHEET	

ELECTRICAL CHARACTERISTICS: SEE NOTES 1, 2, 3, 5, and 7

STANDARD CONDITIONS: VCC= 5.0V TA=OPERATING TEMP. RANGE (UNLESS NOTED).

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Noise Immunity					
For "1"	See note #6	1100	1700		MV
For "0"	See note #6	600	1000		MV
Output Voltage					
"1"	I-Out= 2 mA V-in= 2.7 V	3.8			V
"0"	I-Out= 12.5 mA V-in= 1.2V			0.6	V
	I-Out=7.5mA V-in= 1.2V			0.4	V
Input Current					
Input High	V-in= 2.7V			180	uA
Power Supply Current					
Output High	V-in=4.0V TA=25 C		11.0	14.7	mA
Output Low	V-in-0V TA-25°C		11.2	15.2	mA
Turn on Delay	See test Fig, 1 TA= 25°C		50	80	ns
Turn off Delay	See test Fig, 1 TA= 25°C		40	70	ns
Fan-Out - to sink loads (2.5mA load) - to source loads (180 μ AMPS/LOAD)				5 11	

F.S.C. # 1A-1

F.S.C. # 1A-1

F.S.C. # 1A-1

F.S.C. # 1A-1

F.S.C. # 1A-1

F.S.C. #

SIZE	STANDARD DRAWING NO.	REV
A	05813AL	1A-1
SCALE:	SHEET 3 OF 4	

DO NOT SCALE PRINT

FORM 4313-058-4/68

NOTES:

(1). Pins not specifically referenced are left electrically open.

(2). All Voltage measurements are referenced to the ground pin.

(3). Positive Current flow is defined as current INTO the terminal indicated.

(4). Precautionary measures should be taken to ensure current limiting per the maximum ratings, should the isolation diodes become forward biased.

(5). Positive Logic definition: "Up level = "1" down level = "0".

(6). This characteristics guaranteed by output measurements, F.S.C. #1A-1

(7). Manufacturer reserves the right to make design and process improvements.

(8). Capacitance C includes probe and test jig.

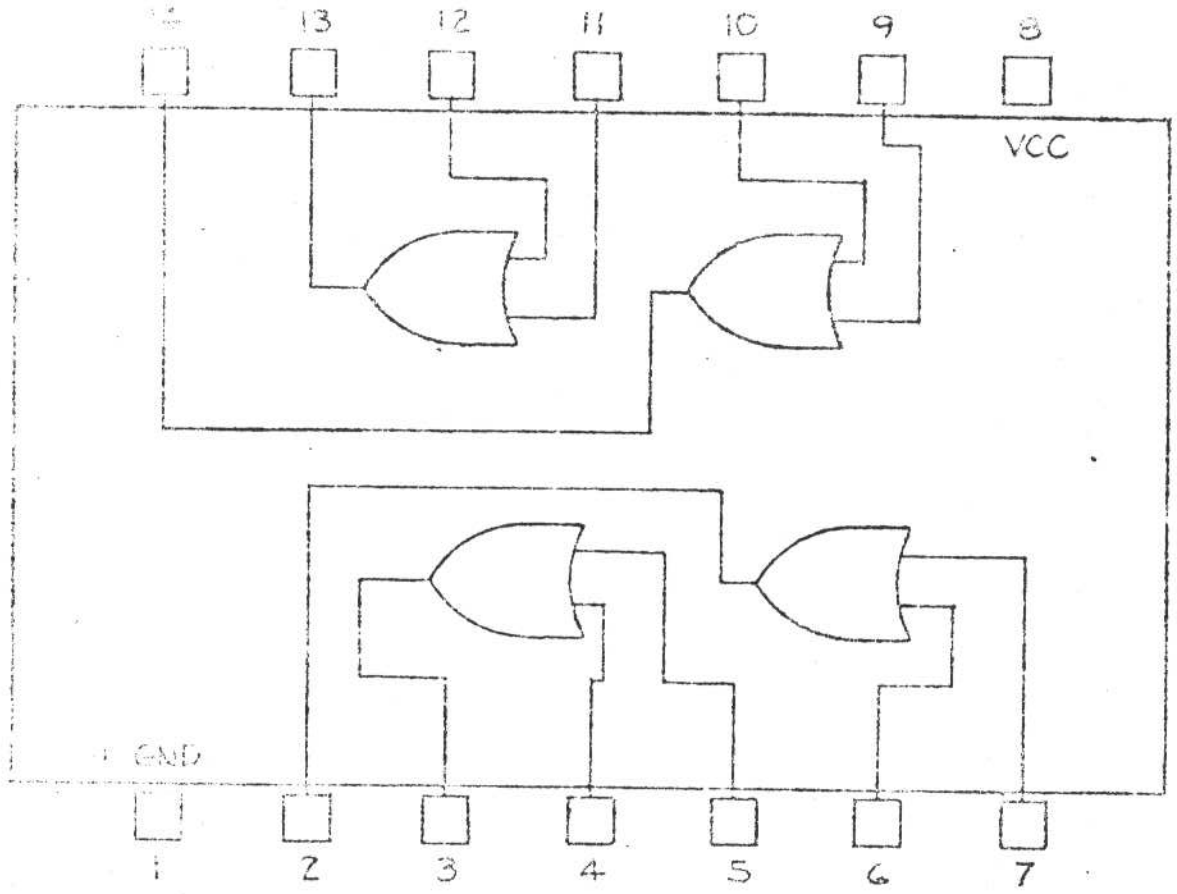
(9). For this test the signal input (Pin 2 or 13) is tied to -6V through 10K Ohm resistor.

(10). Pin 14 must be tied to most negative voltage used.

(11). Standard Source Load is 180uA and Standard Sink Load is -2.8mA.

SIZE	STANDARD MICROCIRCUIT DRAWING NO.	REV
A	03013A1	1A-1

DO NOT SCALE PRINT



384A
PIN CONFIGURATION

FIGURE I

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE		3JUL73	

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package) CERAMIC
Dual 4-Input Positive Nand "Power" Gate

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 4

4. MANUFACTURER'S NAME AND PART NO.

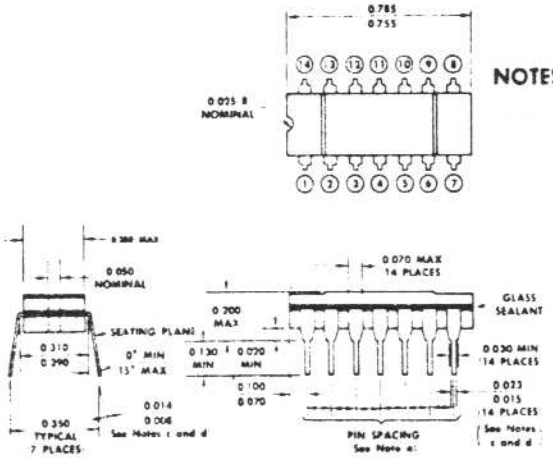
Texas Instrument, Part No. SN7440J
Sprague Part No USN7440AJ
SIGNETICS PART NO. N7440F
Motorola Part No MC7440L

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.		THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
REMOVE BURRS & SHARP EDGES	DRAFTSMAN	DATE	
DIMENSIONS ARE IN INCHES	DESIGNER		TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7440 J
TOLERANCES ON FRACTIONS ± 1/64 DECIMALS ± .005 ANGLES ± 1/2°	CHECKER		
	ENGINEER		
MATERIAL: N/A	RELEASED		SIZE A | SYMBOL B | DRAWING NO. C3313AP | REV A
FINISH: N/A	LOCAL RELEASE		SCALE: NONE | SHEET 1 OF 4

FORM 8083A (6/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

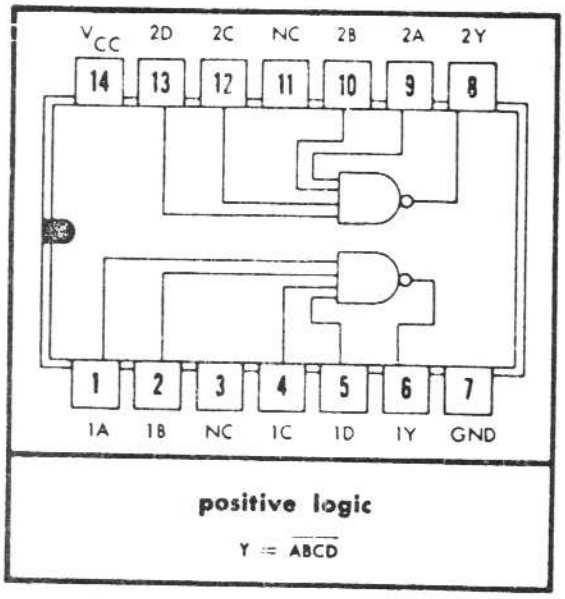
d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

SN7440J

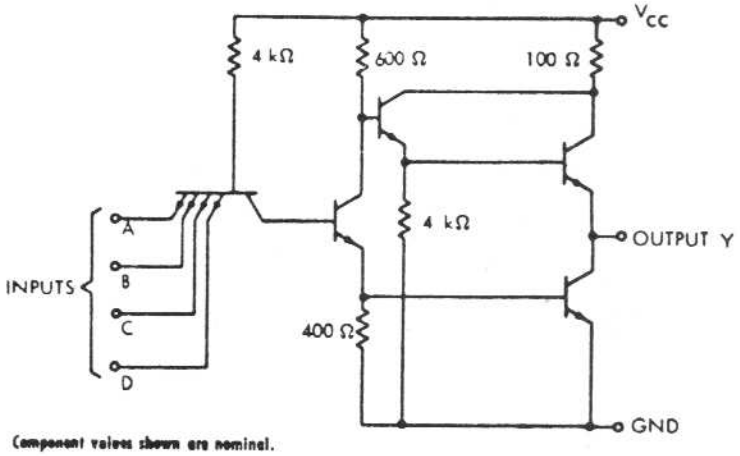
DUAL 4-INPUT POSITIVE NAND BUFFER



positive logic

$Y = \overline{ABCD}$

schematic (each gate)



Component values shown are nominal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Output, N . . . . . 1 to 30

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	V_{CC} = 4.75 V,	$V_{out(0)}$ = 0.4 V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	V_{CC} = 4.75 V,	$V_{out(1)}$ = 2.4 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 V, I_{load} = −1.2 mA	V_{in} = 0.8 V,	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 V, I_{sink} = 48 mA	V_{in} = 2 V,		0.28‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = 5.25 V,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = 5.25 V,	V_{in} = 2.4 V			40	μA
			V_{CC} = 5.25 V,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.25 V		−18		−70	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 5 V		8.6‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 V,	V_{in} = 0		2‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 30$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	C_L = 15 pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	C_L = 15 pF		18	29	ns

†Not more than one output should be shorted at a time.
‡These typical values are at V_{CC} = 5 V, T_A = 25°C.

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE		3JUL73	[illegible]

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package CERAMIC)
Dual "D" Type Flip Flop

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5

4. MANUFACTURER'S NAME AND PART NO.

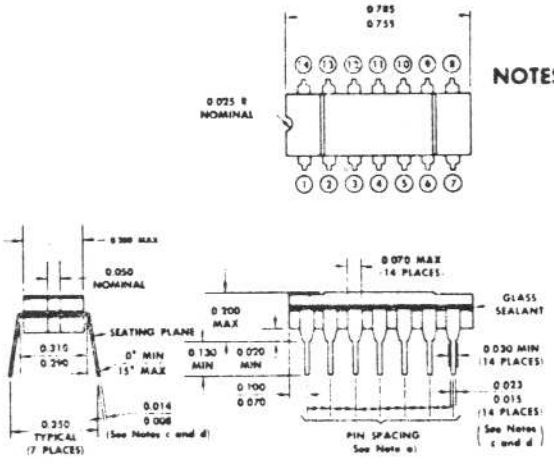
Texas Instrument, Part No. SN7474J
Sprague Part No. USN7474J

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.	FOXBORO	THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
REMOVE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES FINISH DIMS APPLY AFTER PLATING	DRAFTSMAN / DATE	TITLE:	CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7474J
TOLERANCES ON FRACTIONS ± 1/64 DECIMALS ± .005 ANGLES ± 1/2°	DESIGNER		
	CHECKED		
	ENGINEER		
MATERIAL: N/A	RELEASED K	SIZE A	SYMBOL B / DRAWING NO. C3313AQ / REV A
FINISH: N/A	LOCAL RELEASE	SCALE: NONE	SHEET 1 OF 5

FORM 8083A (6/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

description

The SN7474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

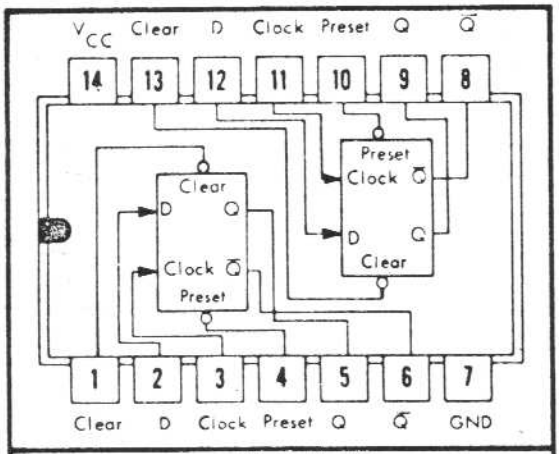
Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed the data input (D) is locked out.

The SN7474 dual flip-flop has the same clocking characteristics as the SN7470 gated (edge-triggered) flip-flop and both are ideally suited for medium- and high-speed applications. The SN7474 can be used at a significant saving in system power dissipation and package count in applications where input gating is not required.

recommended operating conditions

Supply Voltage V_{CC}	4.75 V to 5.25 V
Fan-Out From Each Output, N	1 to 10
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 56)	$\geq$ 30 ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 53)	$\geq$ 30 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 53)	$\geq$ 30 ns

SN7474N
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



positive logic

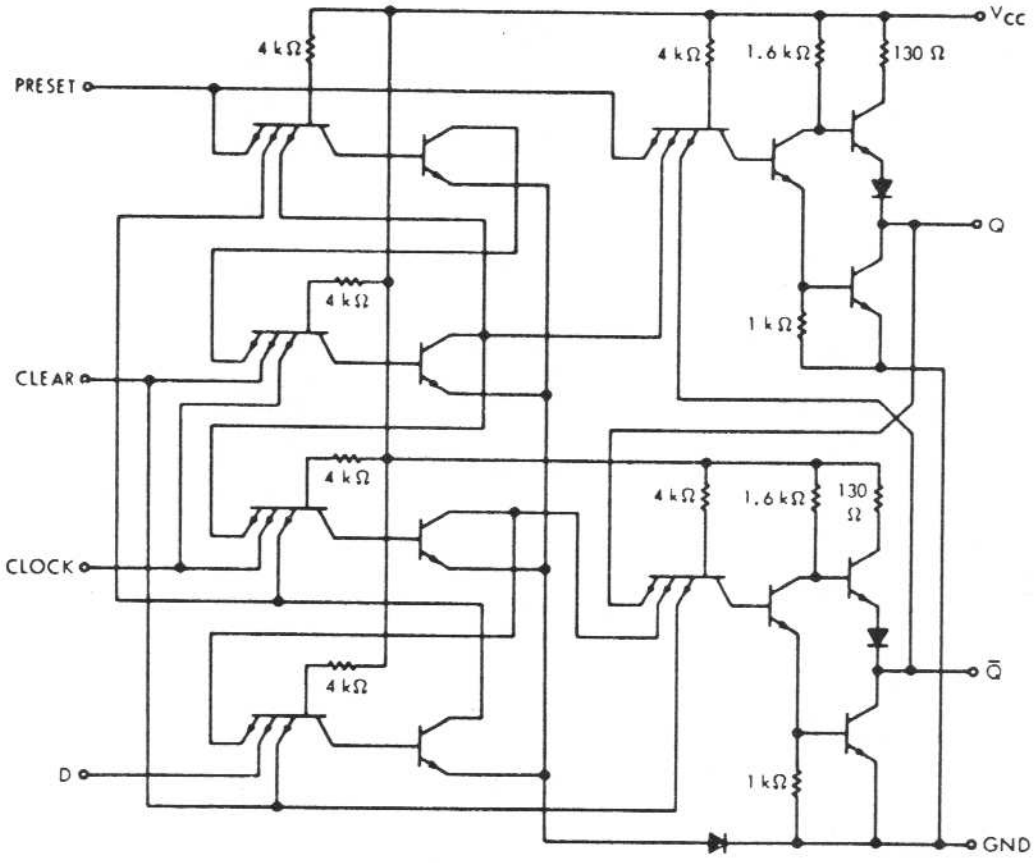
a. Low input to clear sets Q to logical 0.
b. Low input to preset sets Q to logical 1.
c. Clear or preset inputs dominate regardless of clock and D inputs

TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

schematic (each flip-flop)



Component values shown are nominal.

electrical characteristics, $T_A = 0°C$ to 70°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	37	$V_{CC} = 4.75$ V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	37	$V_{CC} = 4.75$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	37	$V_{CC} = 4.75$ V, $I_{load} = -400\ \mu A$	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	38	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	39	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	39	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	40	$V_{CC} = 5.25$ V, $V_{in} = 4.5$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	40	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			80	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	40	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			120	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	41	$V_{CC} = 5.25$ V, $V_{in} = 0$	−18		−57	mA
I_{CC}	Supply current (each flip-flop)	40	$V_{CC} = 5$ V, $V_{in} = 5$ V		8.5‡		mA

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	56	$C_1 = 15$ pF	15	25		MHz
t_{setup}	Minimum input setup time	56	$C_1 = 15$ pF		15	20	ns
t_{hold}	Minimum input hold time	56	$C_1 = 15$ pF		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	52	$C_1 = 15$ pF			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	52	$C_1 = 15$ pF			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	56	$C_1 = 15$ pF	10	20	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	56	$C_1 = 15$ pF	10	28	50	ns

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE		3JUL73	

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package CERAMIC)

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 4

4. MANUFACTURER'S NAME AND PART NO.

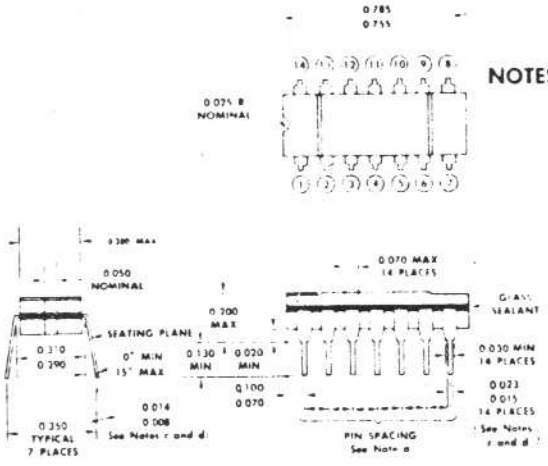
Texas Instrument, Part No. SN7405J
SPRAGUE PART NO. US7405J
MOTOROLA PART NO. MC7405L

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED REMOVE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES ALL DIMS APPLY AFTER PLATING TOLERANCES ON FRACTIONS ± 1/64 DECIMALS ± .005 ANGLES ± 1/2° MATERIAL: N/A FINISH: N/A	WORK AUTH NO.	FOXBORO	THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
	DRAFTSMAN / DATE	TITLE:	CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7405J
	DESIGNER		
	CHECKER		
	ENGINEER		
	RELEASED	SIZE: A	SYMBOL: B
	LOCAL RELEASE	DRAWING NO.: C3313AR	REV: A
		SCALE: N/A	SHEET 1 OF 5

FORM 5083A (6/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

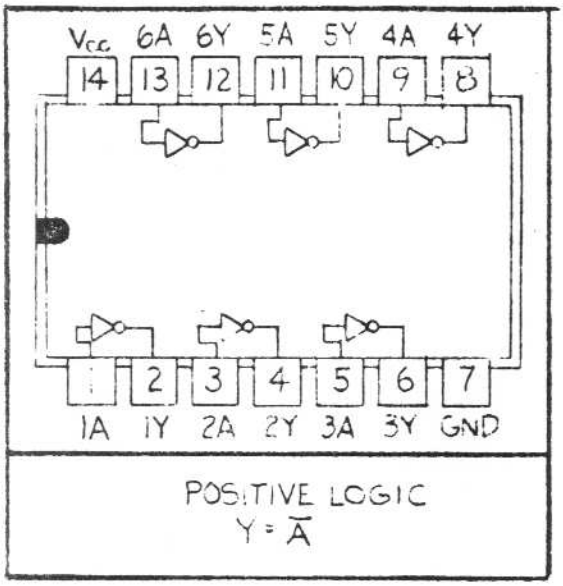
c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

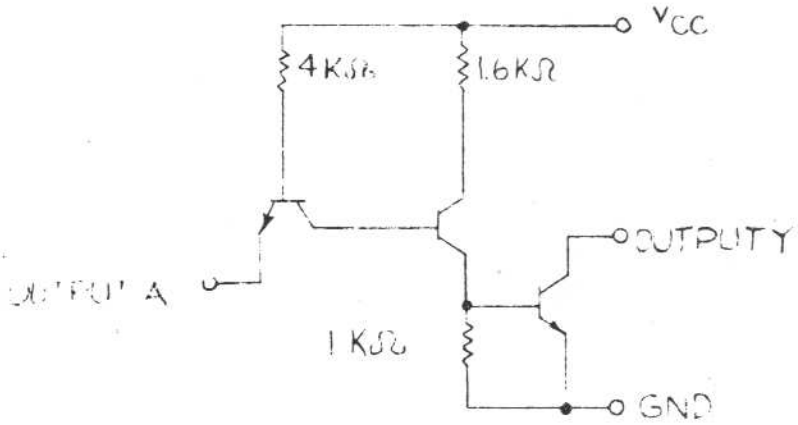
14-PIN FUNCTIONS

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



POSITIVE LOGIC
$Y = \overline{A}$

SCHEMATIC (EACH GATE)



SIZE	SYMBOL	DRAWING NO	REV
A	B	C3313AR	A
SCALE:			SHEET 3 OF 5

DO NOT SCALE PRINT

FORM 50833 (6/67)

DO NOT SCALE PRINT
CAGE 50838 (6/67)

RECOMMENDED OPERATING CONDITIONS
SUPPLY VOLTAGE - 4.75 - 5.25 V

ELECTRICAL CHARACTERISTICS (OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE)

PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN. - TYP.# MAX	UNIT
$V_{IN(I)}$ LOGICAL 1 INPUT VOLTAGE REQ'D AT INPUT TERMINAL TO ENSURE LOGICAL 1 (OFF) LEVEL AT OUTPUT	15	V_{CC} = MIN	2	V
LOGICAL 0 INPUT VOLTAGE REQ'D AT INPUT TERMINAL TO ENSURE LOGICAL 1 (OFF) LEVEL AT OUTPUT	16	V_{CC} = MIN	0.8	V
$I_{OUT(1)}$ OUTPUT REVERSE CURRENT	16	V_{CC} = MIN, V_{IN} = 0.8V, $V_{OUT(1)}$ = 5.5V	250	μA
$V_{OUT(0)}$ LOGICAL 0 OUTPUT VOLTAGE (ON LEVEL)	15	V_{CC} = MIN, V_{IN} = 2V, I_{SINK} = 16 mA	0.4	V
$I_{IN(0)}$ LOGICAL 0 LEVEL INPUT CURRENT	17	V_{CC} = MAX, V_{IN} = 0.4V	-1.6	mA
$I_{IN(1)}$ LOGICAL 1 LEVEL INPUT CURRENT	18	V_{CC} = MAX, V_{IN} = 2.4 V	40	μA
		V_{CC} = MAX, V_{IN} = 5.5 V	1	mA
$I_{CC(0)}$ LOGICAL 0 LEVEL SUPPLY CURRENT	20	V_{CC} = 5V, V_{IN} = 5V, T_A = 25°C	18 33	mA
$I_{CC(1)}$ LOGICAL 1 LEVEL SUPPLY CURRENT	20	V_{CC} = 5V, V_{IN} = 0, T_A = 25°C	6 12	mA

NOTES:
1. † FOR CONDITIONS SHOWN AS MIN OR MAX USE THE APPROPRIATE VALUE SPECIFIED UNDER RECOMMENDED OPERATING CONDITIONS FOR THE APPLICABLE DEVICE TYPE.
2. # THESE TYPICAL VALUES ARE AT V_{CC} = 5V, T_A = 25°C.

SWITCHING CHARACTERISTICS, $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN. - TYP - MAX	UNIT
$T_{PD\emptyset}$ PROPAGATION DELAY TIME TO LOGICAL $\emptyset$ LEVEL	65	$C_L = 15$ PF, $R_L = 400\ \Omega$	8 15	NS
T_{PD1} PROPAGATION DELAY TIME TO LOGICAL 1 LEVEL.	65	$C_L = 15$ PF, $R_L = 4\ \Omega$	40 55	NS

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50838 (6/67)

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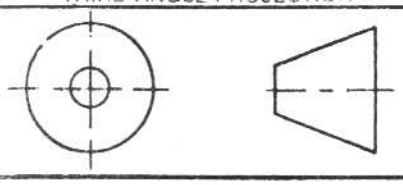
THIRD ANGLE PROJECTION



REVISIONS	SYM	CHANGE NO.	DATE	APP
	A	LOCAL RELEASE	3JUL73	

PL C3001 X X

FIRST USED ON

GR

APPLICATION

DO NOT SCALE DRAWING

1. DESCRIPTION

Circuit, integrated (dual in-line package) mono stable multivibrator (CERAMIC)

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 4

4. MANUFACTURER'S NAME & PART NO.

Texas Instruments Part No. SN74121J
SIGNETICS PART NO. N74121F

PRINT DISTR	
DEPT	QTY

FOR PARTS LIST SEE DWG PL

TOLERANCES UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

.X ± | .XX ±.04 | .XXX ±.010

ANGLES ± | FRACTIONS ± | ⊕ .028 DIA

MATL

FINISH

		DATE
DRAWN		
CHECKED		
DESIGNED		
DRAFTING		
RESTRICTED RELEASE		
LOCAL RELEASE		2JUL73
CORPORATE RELEASE		

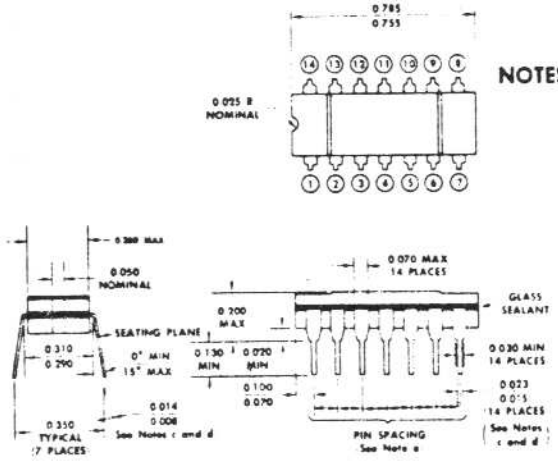
THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
Circuit, Integrated
Dual In-line Package
Type SN74121J

SIZE	DWG CODE	DRAWING NUMBER	REV
A	B	C3313AS	A

SCALE | WT | SHEET 1 OF 4

FORM 5877 [11/69]



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

CIRCUIT TYPES SN54121, SN74121
MONOSTABLE MULTIVIBRATORS

logic

TRUTH TABLE (See Notes 1 thru 3)

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	Inhibit
0	X	1	0	X	0	Inhibit
X	0	1	X	0	0	Inhibit
0	X	0	0	X	1	One Shot
X	0	0	X	0	1	One Shot
1	1	1	X	0	1	One Shot
1	1	1	0	X	1	One Shot
X	0	0	X	1	0	Inhibit
0	X	0	1	X	0	Inhibit
X	0	1	1	1	1	Inhibit
0	X	1	1	1	1	Inhibit
1	1	0	X	0	0	Inhibit
1	1	0	0	X	0	Inhibit

$1 = V_{in(1)} \geq 2\ V$

$0 = V_{in(0)} \leq 0.8\ V$

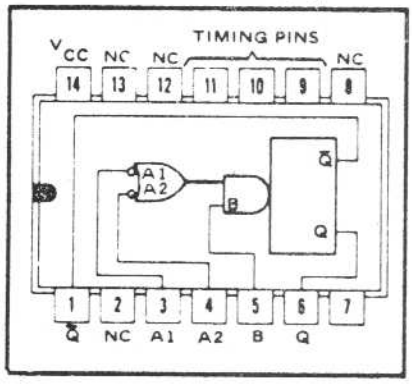
NOTES: 1. t_n = time before input transition.

2. t_{n+1} = time after input transition.

3. X indicates that either a logical 0 or 1 may be present.

4. NC = No Internal Connection.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)
(SEE NOTES 6 THRU 9)



5. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.

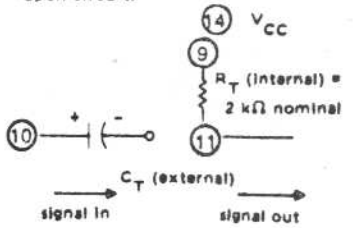
6. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table)

7. External timing capacitor may be connected between pin (10) (positive) and pin (11). With no external capacitance, an output pulse width of typically 30 ns is obtained.

8. To use the internal timing resistor (2 kΩ nominal), connect pin (9) to pin (14).

9. To obtain variable pulse width connect external variable resistance between pin (9) and pin (14). No external current limiting is needed.

10. For accurate repeatable pulse widths connect an external resistor between pin (11) and pin (14) with pin (9) open-circuit.



SIZE	SYMBOL	DRAWING NO.	REV
A	B	C3313AS	A
SCALE:		SHEET 3 OF 4	

DO NOT SCALE PRINT

FORM 5083B (6/67)

CIRCUIT TYPES SN54121, SN74121
MONOSTABLE MULTIVIBRATORS

electrical characteristics over operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNITS
V_{T+}	Positive-going threshold voltage at A input	57	V_{CC} = MIN			1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	57	V_{CC} = MIN		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	57	V_{CC} = MIN			1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	57	V_{CC} = MIN		0.8	1.35		V
$V_{out(0)}$	Logical 0 output voltage	57	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$V_{out(1)}$	Logical 1 output voltage	57	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.3		V
$I_{in(0)}$	Logical 0 level input current at A1 or A2	58	V_{CC} = MAX, V_{in} = 0.4 V			−1	−1.6	mA
$I_{in(0)}$	Logical 0 level input current at B	59	V_{CC} = MAX, V_{in} = 0.4 V			−2	−3.2	mA
$I_{in(1)}$	Logical 1 level input current at A1 or A2	60	V_{CC} = MAX, V_{in} = 2.4 V			2	40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			0.05	1	mA
$I_{in(1)}$	Logical 1 level input current at B	61	V_{CC} = MAX, V_{in} = 2.4 V			4	80	μA
			V_{CC} = MAX, V_{in} = 5.5 V			0.05	1	mA
I_{OS}	Short circuit output current at Q or $\overline{Q}$§	62 and 63	V_{CC} = MAX	SN54121	−20	−25	−55	mA
				SN74121	−18	−25	−55	
I_{CC}	Power supply current in quiescent (unfired) state	64	V_{CC} = MAX			13	25	mA
I_{CC}	Power supply current in fired state	64	V_{CC} = MAX			23	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd1}	Propagation delay time to logical 1 level from B input to Q output	72	C_L = 15 pF,	C_T = 80 pF	15	35	55	ns
t_{pd1}	Propagation delay time to logical 1 level from A1/A2 inputs to Q output				25	45	70	ns
t_{pd0}	Propagation delay time to logical 0 level from B input to $\overline{Q}$ output	72	C_L = 15 pF,	C_T = 80 pF	20	40	65	ns
t_{pd0}	Propagation delay time to logical 0 level from A1/A2 inputs to $\overline{Q}$ output				30	50	80	ns
$t_{p(out)}$	Pulse width obtained using internal timing resistor	73	C_L = 15 pF, R_T = Open,	C_T = 80 pF, Pin ⑨ to V_{CC}	70	110	150	ns
$t_{p(out)}$	Pulse width obtained with zero timing capacitance	73	C_L = 15 pF, R_T = Open,	C_T = 0, Pin ⑨ to V_{CC}	20	30	50	ns
$t_{p(out)}$	Pulse width obtained using external timing resistor	73	C_L = 15 pF, R_T = 10 kΩ,	C_T = 100 pF, Pin ⑨ Open	600	700	800	ns
			C_L = 15 pF, R_T = 10 kΩ,	C_T = 1 μF, Pin ⑨ Open	6	7	8	ms
t_{hold}	Minimum duration of trigger pulse	73	C_L = 15 pF, R_T = Open,	C_T = 80 pF, Pin ⑨ to V_{CC}		30	50	ns

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY / APPROVED BY
A	RESTRICTED RELEASE			

REV STATUS OF SHEETS	REV	A	A	A													
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .005
ANGLES ± 1°

DRAWN | CHK'D | DATE
DRAFTING
DESIGNED E. [illegible]

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
INTEGRATED CIRCUIT US7439H
QUAD-2INPUT NAND BUFFER GATE-OPEN
COLLECTOR OUTPUT

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED [illegible]
QUAL
ENGR

SIZE A

DRAWING NUMBER C3313AT

ASSIGNED FOR

CONTRACT

SCALE

WT

SHEET 1 OF 3

FM 5758-C (5/69)

1.0 DESCRIPTION Integrated Circuit US7439H

Quad-2-Input NAND Buffer Gate-Open Collector Output

2.0 PHYSICAL CHARACTERISTICS

Dual-In-Line Package 14-Pin
Hermetically Sealed.
See fig # 1

3.0 PERFORMANCE CHARACTERISTICS

Diode Clamping on all Inputs
Low Power Dissipation
High Noise Margin: 1 Volt
Supply Voltage Vcc: 5 Volts ± 5%
Operating Temp. Range: 0°C to + 70°C

4.0 QUALITY ASSURANCE PROVISIONS

Inspect per this drawing

5.0 MANUFACTURER'S NAME AND PART NUMBER

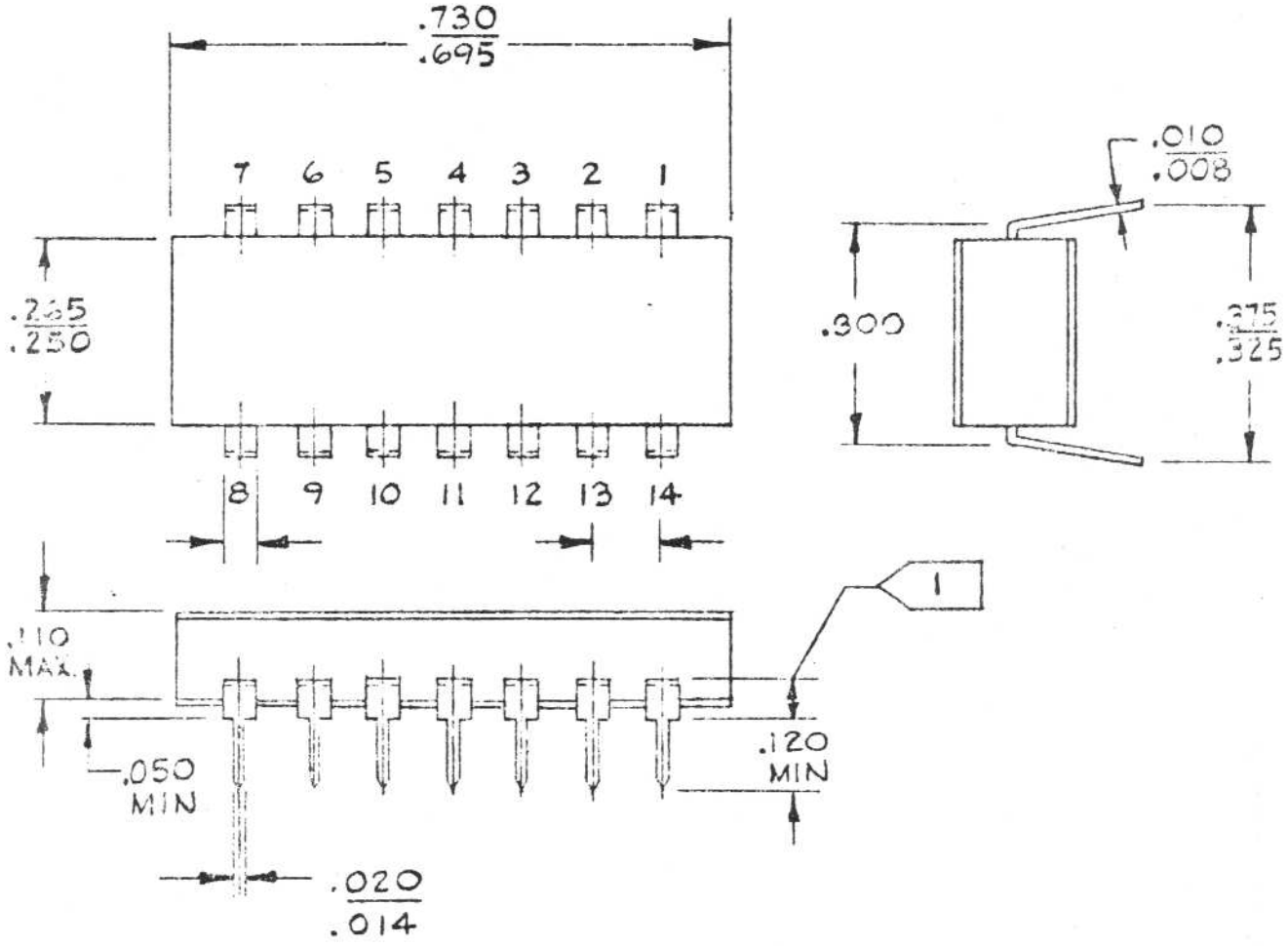
SPRAGUE, Electric Company
North Adams, Mass

P/N # US7439H

SIZE	SYMBOL	DRAWING NO.	REV
A		C3313AT	1A

DO NOT SCALE PRINT

SCALE: SHEET 2 OF 3



NOTES:

1. LEAD SPACING SHALL BE MEASURED WITHIN THIS ZONE.
2. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.

FIGURE I

SIZE	SYMBOL DRAWING NO.	REV
A	C3313AT	1A
DO NOT SCALE PRINT	SCALE: NONE	SHEET 3 OF 3

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN 1912			

REV STATUS OF SHEETS																	
REV	A	A	A	A	A												
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

DRAWN B. WALKER / CHK'D E. WALKER	DATE 3/24/69	
DRAFTING		
DESIGNED		
APPROVED J. P. DENSLER	3/24/69	
LOCAL RELEASE M. J. COOK	5/14/69	
CORPORATE RELEASE B. FRANKLIN	JUNE 73	

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT, INTEGRATED
DUAL IN-LINE PACKAGE
TYPE 7400N

SUPERSEDING
INTERCHANGEABLE SIMILAR TO YES NO

DESIGNED FOR

SIZE A | B

DRAWING NUMBER V3008EA

SCALE | WT | SHEET 1 OF 5

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Quadruple 2-Input Positive Nand Gate

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5.

4. MANUFACTURER'S NAME AND PART NUMBER

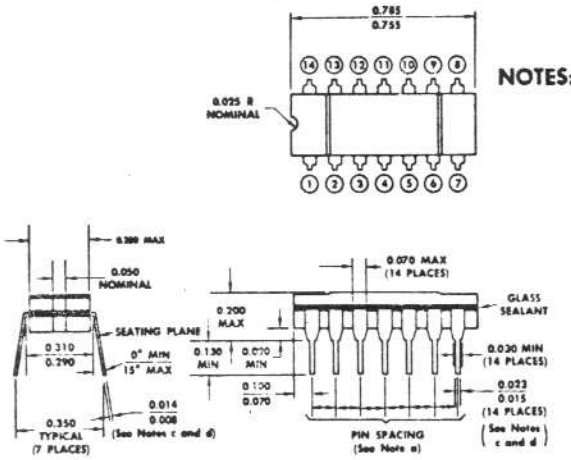
Texas Instrument, Part No. SN7400N
Sprague Part No. USN7400A
National Semi-conductor Corp. Part No. DM8000N
Motorola Part No. MC7400P

NOTE: Only the item described on this drawing when procurred from the mfg. listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	V3008EA	A
SCALE:		SHEET 2 OF	

DO NOT SCALE PRINT

FORM A816-088-4/68



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

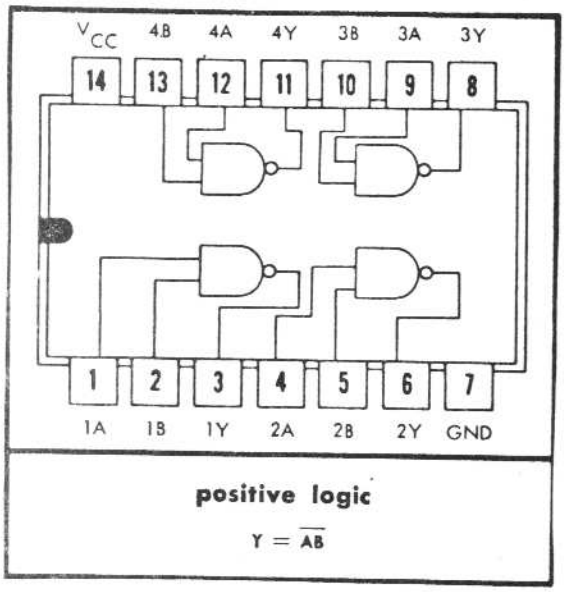
c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

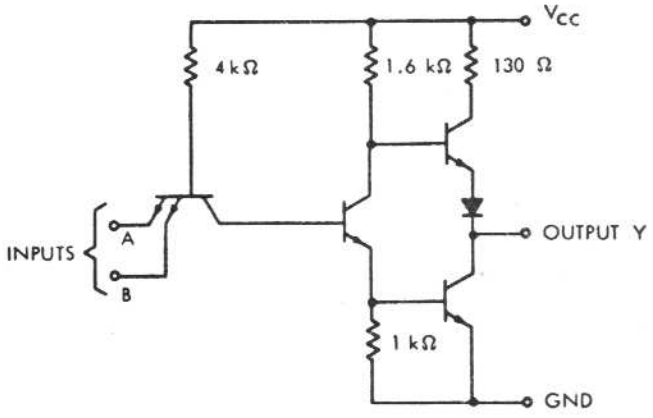
SN7400N
QUADRUPLE 2-INPUT POSITIVE NAND GATE



positive logic

$Y = \overline{AB}$

schematic (each gate)



Component values shown are nominal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . . 1 to 10

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.75$ V,	$V_{out(0)} \leq 0.4$ V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.75$ V,	$V_{out(1)} \geq 2.4$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	$V_{CC} = 4.75$ V, $I_{load} = -400\ \mu A$	$V_{in} = 0.8$ V,	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA	$V_{in} = 2$ V,		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	$V_{CC} = 5.25$ V,	$V_{in} = 0.4$ V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	$V_{CC} = 5.25$ V,	$V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V,	$V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	5	$V_{CC} = 5.25$ V,		−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	$V_{CC} = 5$ V,	$V_{in} = 5$ V		3‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	$V_{CC} = 5$ V,	$V_{in} = 0$		1‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	$C_l = 15$ pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	$C_l = 15$ pF		18	29	ns

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	Local Release ECN 1912			

REV STATUS OF SHEETS																	
REV	A	A	A	A	A	A	A										
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
DRAFTING	B. WALKER	B. WALKER	3/24/69
DESIGNED			

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
Circuit, Integrated
Dual In-Line Package
Type SN7401N

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED	J. P. DENSLER	3/24/69
LOCAL RELEASE	M. J. COOK	5/11/69
CORPORATE RELEASE	B. FRANKLIN	5/28/69

DESIGNED FOR

SIZE A | B

DRAWING NUMBER V3008EB

SCALE | WT | SHEET 1 OF 7

FORM 5758-C (5/69)

1.0 DESCRIPTION:

Circuit, Integrated (Dual In-Line Package)
Quad 2-Input Nano Gate W/Open Collector Output

2.0 PHYSICAL CHARACTERISTICS:

2.1 See Sheet 3.

3.0 PERFORMANCE CHARACTERISTICS:

3.1 See Sheets 5, 6, & 7.

4.0 QUALITY ASSURANCE PROVISIONS:

Inspect per this drawing.

Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without engineering approval.

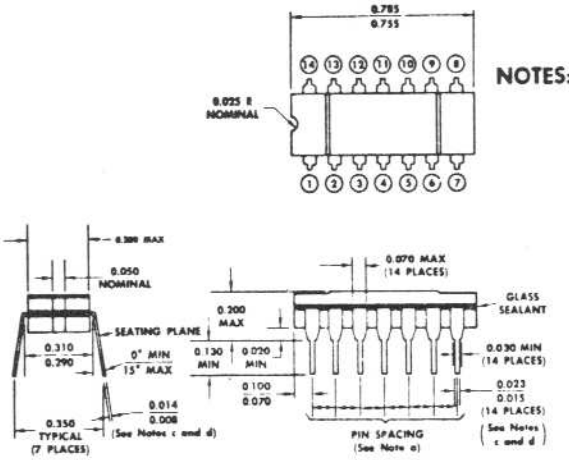
5.0 VENDOR'S NAME AND PART NO.:

Texas Instrument, Part No. SN7401N
Sprague Part No. USN7401A
Motorola Part No. MC7401P

SIZE	SYMBOL	DRAWING NO.	REV
A	B	V3008EB	A
	SCALE:		SHEET 2 OF

DO NOT SCALE PRINT

FORM A816-888-4/66



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

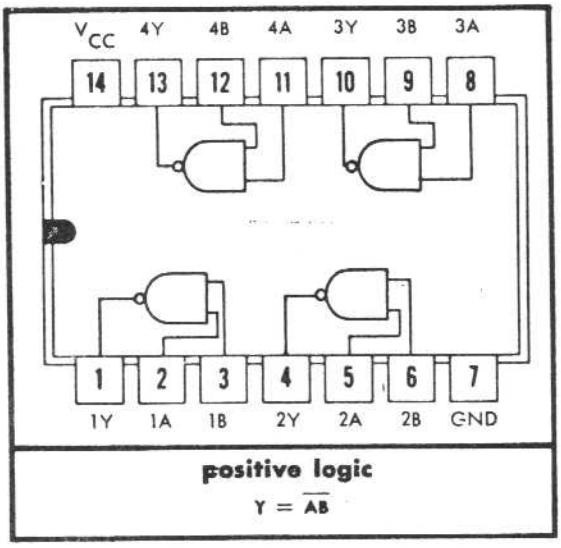
d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

SN7401N

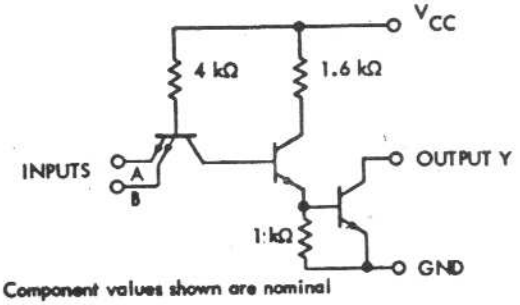
QUADRUPLE 2-INPUT POSITIVE NAND GATE (WITH OPEN-COLLECTOR OUTPUT)



positive logic

$Y = \overline{AB}$

schematic (each gate)



Component values shown are nominal

THE FOXBORO COMPANY SYSTEMS DIVISION	B V3008 EB	Rev.
	Sheet 4 of	

Form 5039 (6/68)

APPLICATION DATA

combined fan-out and wire-OR capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-OR function, and simultaneously, will drive from one to nine TTL loads. When no other open-collector gates are paralleled, this gate may be used to drive ten TTL loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and I_{off} current (through paralleled outputs) will be available during a logical 1 level at the output. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the logical 0 level even if one of the paralleled outputs is sinking all the current.

In both conditions (logical 0 and logical 1) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where: V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

logical 1 (off level) circuit calculations (see figure E1)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the $V_{out(1)}$ level required at the load:

$$V_{RL} = V_{CC} - V_{out(1)} \text{ required}$$

The total current through the load resistor (I_{RL}) is the sum of the load currents ($I_{in(1)}$) and off-level reverse currents ($I_{out(1)}$) through each of the wire-OR connected outputs:

$$I_{RL} = \eta \cdot I_{out(1)} + N \cdot I_{in(1)} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{out(1)} \text{ required}}{\eta \cdot I_{out(1)} + N \cdot I_{in(1)}}$$

where: η = number of gates wire-OR connected, and N = number of TTL loads.

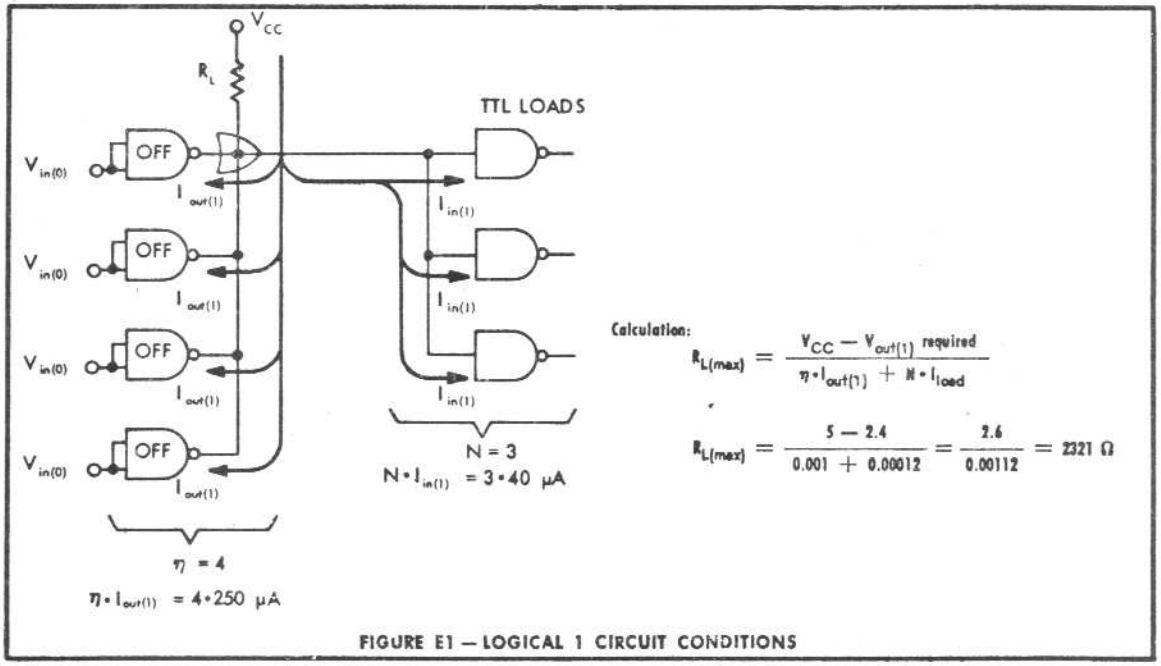


FIGURE E1 — LOGICAL 1 CIRCUIT CONDITIONS

APPLICATION DATA

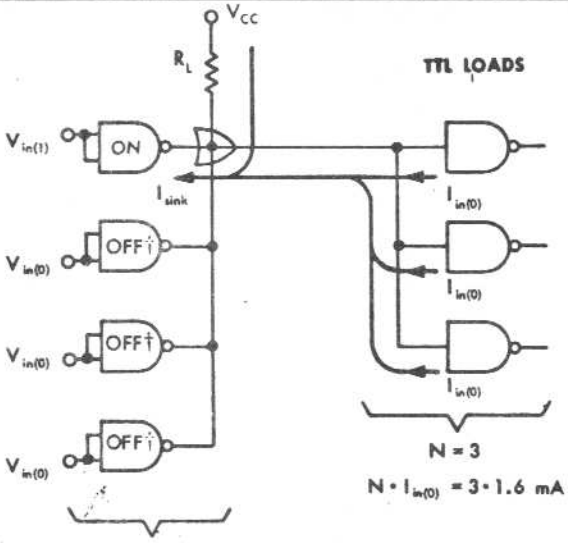
logical 0 (on level) circuit calculations (see figure E2)

The current through the resistor must be limited to the maximum sink-current capability of one output transistor. Note that if several output transistors are wire-OR connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during logical 0 periods, the current must be limited to 16 mA, the maximum current which will ensure a logical 0 maximum of 0.4 volts.

Also, fan-out must be considered. Part of the 16 mA will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)\ required}}{I_{sink}\ capability - I_{sink}\ from\ TTL\ loads}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{out(0)\ required}}{I_{sink}\ capability - I_{sink}\ from\ TTL\ loads}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.016 - 0.0048} = \frac{4.6}{0.0112} = 410\ \Omega$$

†Current through OFF outputs is negligible at logical 0.

FIGURE E2 — LOGICAL 0 CIRCUIT CONDITIONS

driving TTL loads and combining outputs

Table 1 provides minimum and maximum resistor values, calculated from equations shown above, for driving one to ten TTL loads and wire-OR connecting two to seven parallel outputs. Each value shown for wire-OR output one is determined by the fan-out plus the leakage of a single output transistor. Extension beyond seven wire-OR connections is permitted with fan-outs of seven or less if a valid minimum and maximum R_L is possible. When fanning-out to ten TTL loads the calculation for the minimum value of R_L indicates that an infinite resistance should be used ($V_{RL} \div 0 = \infty$;) however, the use of a 4-kΩ resistor in this case will satisfy the logical 1 condition and limit the logical 0 level to less than 0.43 V.

TABLE 1

FAN-OUT TO TTL LOADS	WIRE-OR OUTPUTS							
	1	2	3	4	5	6	7	1 to 7
1	8965	4814	3291	2500	2015	1688	1452	319
2	7878	4482	3132	2407	1954	1645	1420	359
3	7027	4193	2988	2321	1897	1604	1390	410
4	6311	3939	2857	2241	1843	1566	1361	479
5	5777	3714	2736	2166	1793	1529	1333	575
6	5306	3513	2626	2096	1744	1494	1306	718
7	4905	3333	2524	2031	1699	1460	1280	958
8	4561	3170	2429	1969	1656	X	X	1437
9	4262	3023	X	X	X	X	X	2875
10	4000	X	X	X	X	X	X	∞‡
	MAXIMUM							MIN
	LOAD RESISTOR VALUE IN OHMS							

X — Not recommended or not possible.

‡ — The theoretical value is ∞. See explanation in text.

All values shown in the table are based on:

Logical 1 conditions: $V_{CC} = 5$ V, $V_{out(1)\ required} = 2.4$ V

Logical 0 conditions: $V_{CC} = 5$ V, $V_{out(0)\ required} = 0.4$ V

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . . 1 to 10

electrical characteristics, $T_A = 0°C$ to 70°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.75$ V, $V_{out(0)} \leq 0.4$ V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.75$ V, $V_{out(1)} \geq 2.4$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	$V_{CC} = 4.75$ V, $V_{in} = 0.8$ V, $I_{load} = -400\ \mu A$	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	$V_{CC} = 4.75$ V, $V_{in} = 2$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	5	$V_{CC} = 5.25$ V,	−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	$V_{CC} = 5$ V, $V_{in} = 5$ V		3‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	$V_{CC} = 5$ V, $V_{in} = 0$		1‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	$C_L = 15$ pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	$C_L = 15$ pF		18	29	ns

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
B	ECN 3121		10 APR 70	W.J.J.

REV STATUS OF SHEETS																	
REV	B	B															
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

DRAWN B. WALKER	CHK'D B. WALKER	DATE 3/24/69
DRAFTING		
DESIGNED		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT, INTEGRATED
DUAL IN-LINE PACKAGE
TYPE SN7402N

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED J.P. DENSLER	3/24/69	
LOCAL RELEASE M.N. COOK	5/11/69	
CORPORATE RELEASE B. FRANKLIN	7/11/69	

DESIGNED FOR

SIZE		DRAWING NUMBER
A	B	V3008EC
SCALE	WT	SHEET 1 OF 2

FORM 5758-C (5/69)

DESCRIPTION

Circuit, Integrated
Quad 2-Input Nor Gate

PHYSICAL CHARACTERISTICS

14 Pin Dual in-line package
For more detailed physical characteristics see mfg.'s catalog.

PERFORMANCE CHARACTERISTICS

Supply Voltage Vcc: 4.75V to 5.25V
Fan Out: 1 to 10
Ambient Temperature: 0°C to 70°C
For more detailed performance characteristics see mfg.'s catalog,

QUALITY ASSURANCE PROVISIONS

Inspect per parameters outlined in mfg.'s catalog.

MANUFACTURER'S NAME AND PART NUMBER

Texas Instrument: SN7402N
Sprague: USN7402A
Motorola: MC7402P

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	V3008EC	B
		SCALE:	SHEET 2 OF 2

DO NOT SCALE PRINT

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN 1912			

REV STATUS OF SHEETS	REV	A	A	A	A	A											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

DRAWN E. WALKER	CHK'D E. WALKER	DATE 3/24/69
DRAFTING		
DESIGNED		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT INTEGRATED
DUAL IN-LINE PACKAGE
SN7410N

SUPERSEDING INTERCHANGEABLE SIMILAR TO YES NO	APPROVED J. P. DeMoore	3/24/69	
	LOCAL RELEASE M. J. Cook	3/11/69	
DESIGNED FOR	CORPORATE RELEASE S. Feinsilver	3/13/69	

SIZE		DRAWING NUMBER
A	B	V3008EE
SCALE	WT	SHEET 1 OF 5

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Triple 3-Input Positive Nand Gate

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5.

4. MANUFACTURER'S NAME AND PART NO.

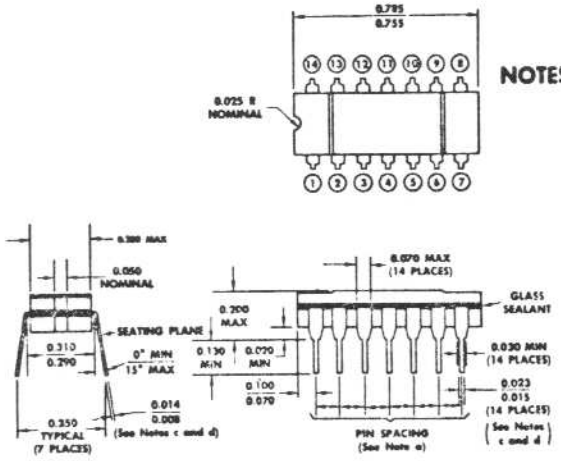
Texas Instrument, Part No. SN7410N
Sprague Part No. USN7410A
National Semi-conductor Corp. Part No. DM8010N
Motorola Part No. MC7410P

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE	SYMBOL	DRAWING NO.	REV
A		V3003E	A
		SCALE:	SHEET 1 OF

DO NOT SCALE PRINT

FORM A818-088-4/66



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

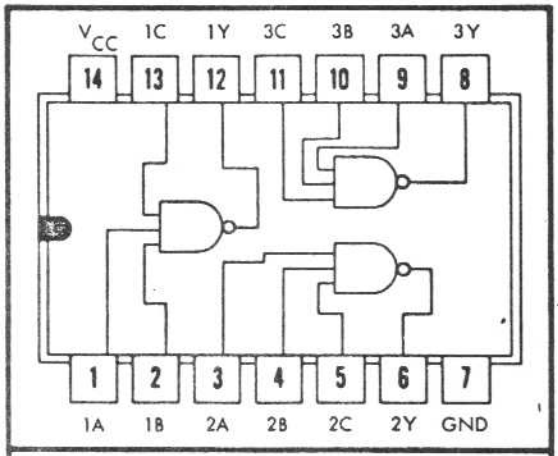
c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

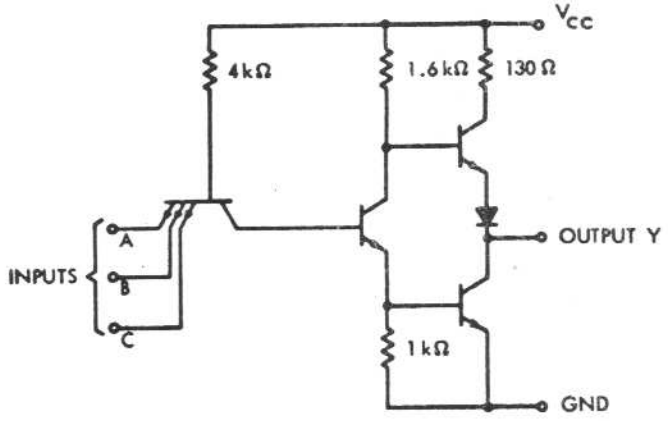
SN7410N
TRIPLE 3-INPUT POSITIVE NAND GATE



positive logic

$Y = \overline{ABC}$

schematic (each gate)



Component values shown are nominal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Output, N . . . . . 1 to 10

electrical characteristics, $T_A = 0°C$ to 70°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.75$ V, $V_{out(0)} \leq 0.4$ V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.75$ V, $V_{out(1)} \geq 2.4$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	$V_{CC} = 4.75$ V, $V_{in} = 0.8$ V, $I_{load} = -400\ \mu A$	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	$V_{CC} = 4.75$ V, $V_{in} = 2$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	5	$V_{CC} = 5.25$ V	−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	$V_{CC} = 5$ V, $V_{in} = 5$ V		3‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	$V_{CC} = 5$ V, $V_{in} = 0$		1‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	$C_l = 15$ pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	$C_l = 15$ pF		18	29	ns

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN 1912			

REV STATUS OF SHEETS	REV	A	A	A	A	A											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

DRAWN R. WALLEN	CHK'D R. WALLEN	DATE 3/26/71
DRAFTING		
DESIGNED		
APPROVED J.P. Dennis		3/26/71
LOCAL RELEASE M.J. Clark		7/16/71
CORPORATE RELEASE [illegible]		7/15/71

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT, INTEGRATED
DUAL IN-LINE PACKAGE
TYPE SN7420N

SUPERSEDING
INTERCHANGEABLE SIMILAR TO YES NO

DESIGNED FOR

SIZE A | B

DRAWING NUMBER V3008EF

SCALE | WT | SHEET 1 OF 5

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Dual 4-Input Positive Gate

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5.

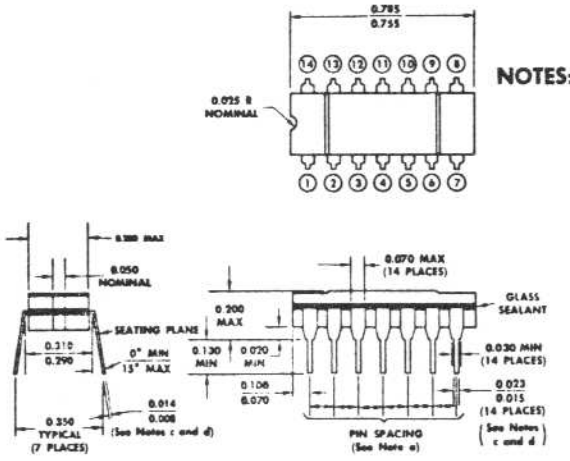
4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7420N
Sprague Part No. USN7420A
National Semi-conductor Corporation DM8020N

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use, A substitute item shall not be used without Engineering approval.

SIZE	SYMBOL	DRAWING NO.	REV
A	D	V3008EF	A
SCALE:		SHEET 2 OF	

DO NOT SCALE PRINT



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

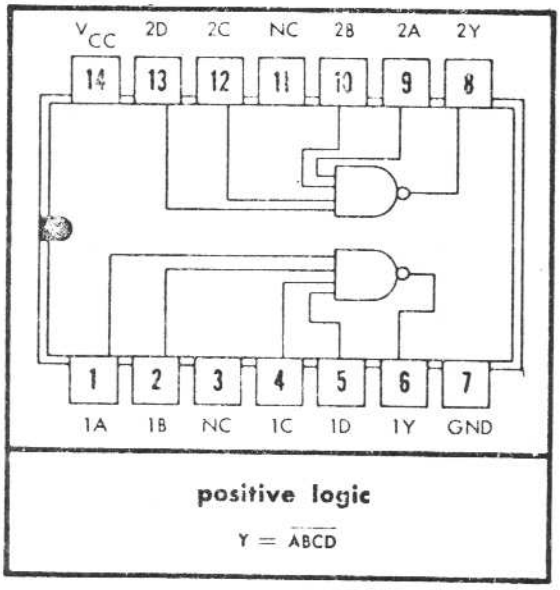
c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

SN7420N
DUAL 4-INPUT POSITIVE NAND GATE

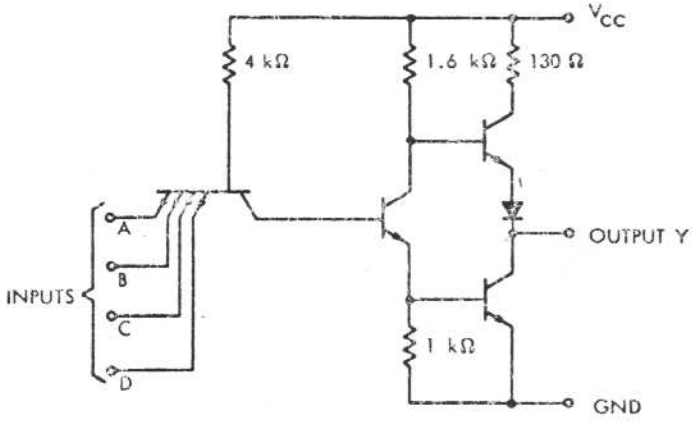


positive logic

$Y = \overline{ABCD}$

NC — No internal connection.
†Patented by Texas Instruments

schematic (each gate)



Component values shown are nominal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . . 1 to 10

electrical characteristics, $T_A = 0°C$ to 70°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.75$ V,	$V_{out(0)} \leq 0.4$ V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.75$ V,	$V_{out(1)} \geq 2.4$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	$V_{CC} = 4.75$ V, $I_{load} = -400\ \mu A$	$V_{in} = 0.8$ V,	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA	$V_{in} = 2$ V,		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	$V_{CC} = 5.25$ V,	$V_{in} = 0.4$ V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	$V_{CC} = 5.25$ V,	$V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V,	$V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	5	$V_{CC} = 5.25$ V		−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	$V_{CC} = 5$ V,	$V_{in} = 5$ V		3‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	$V_{CC} = 5$ V,	$V_{in} = 0$		1‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	$C_l = 15$ pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	$C_l = 15$ pF		18	29	ns

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN NO. 1912			

REV STATUS OF SHEETS	REV	A	A	A	A	A											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
DRAFTING	E. WALKER	E. WALKER	3/16/70
DESIGNED			

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT, INTEGRATED
DUAL IN-LINE PACKAGE
TYPE SN7430N

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED	J. P. Duncan	3/24/70
LOCAL RELEASE	M. V. Cook	5/11/70
CORPORATE RELEASE	E. FRANKLIN	5/13/70

DESIGNED FOR

SIZE A | B | DRAWING NUMBER V3008EK

SCALE | WT | SHEET 1 OF 5

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
8-Input Positive Nand Gate

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5.

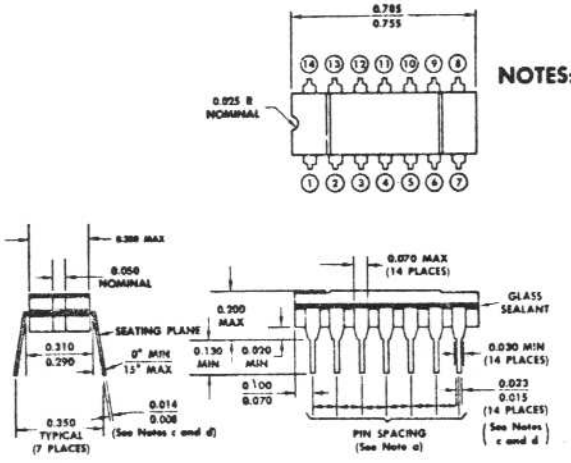
4. MANUFACTURER'S ANME AND PART NO.

Texas Instrument, Part No. SN7430N
Sprague Part No. USN7430A
Motorola Part No. MC7430P

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	V3008EK	A
		SCALE:	SHEET 2 OF

DO NOT SCALE PRINT



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

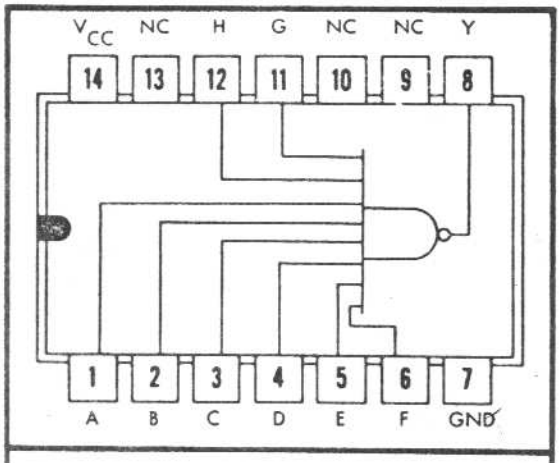
e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

THE FOXBORO COMPANY SYSTEMS DIVISION	B	V3008EK	Rev. A
		Sheet 3 of	

Form 5039 (6/68)

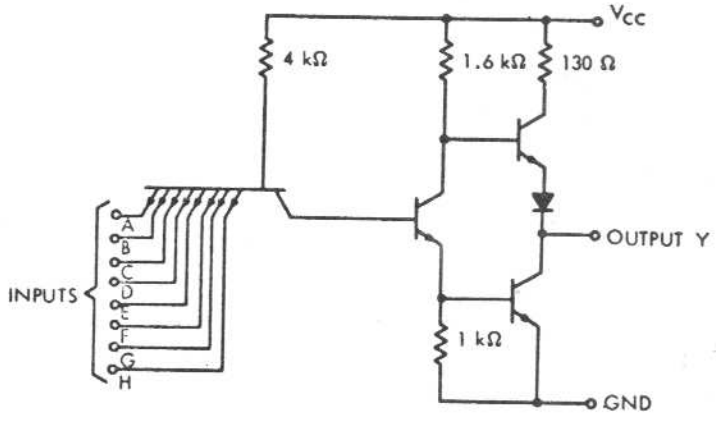
SN7430N
8-INPUT POSITIVE NAND GATE



positive logic

$Y = \overline{ABCDEFGH}$

schematic



Component values shown are nominal.

THE FOXBORO COMPANY SYSTEMS DIVISION	B V3003EK	Rev. A
	Sheet 4 of	

Form 5039 (6/68)

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . . 1 to 10

electrical characteristics, $T_A = 0°C$ to 70°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.75$ V, $V_{out(0)} \leq 0.4$ V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.75$ V, $V_{out(1)} \geq 2.4$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	$V_{CC} = 4.75$ V, $V_{in} = 0.8$ V, $I_{load} = -400\ \mu A$	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	$V_{CC} = 4.75$ V, $V_{in} = 2$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	5	$V_{CC} = 5.25$ V	−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	$V_{CC} = 5$ V, $V_{in} = 5$ V		3‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	$V_{CC} = 5$ V, $V_{in} = 0$		1‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	$C_l = 15$ pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	$C_l = 15$ pF		18	29	ns

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	ECN 1912			

REV STATUS OF SHEETS	REV	A	A	A	A	A											
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

DRAWN B.W.	CHK'D B. W.	DATE 3/24/69
DRAFTING BRICE WALKER		3/24/69
DESIGNED		
APPROVED J. P. DENSLER		3/24/69
LOCAL RELEASE M. COOK		5/1/69
CORPORATE RELEASE B. FRANKLIN		9/21/73

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7440N

SUPERSEDING
INTERCHANGEABLE SIMILAR TO YES NO

DESIGNED FOR

SIZE		DRAWING NUMBER
A	B	V3008EL
SCALE	WT	SHEET 1 OF 5

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Dual 4-Input Positive Nand "Power" Gate

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

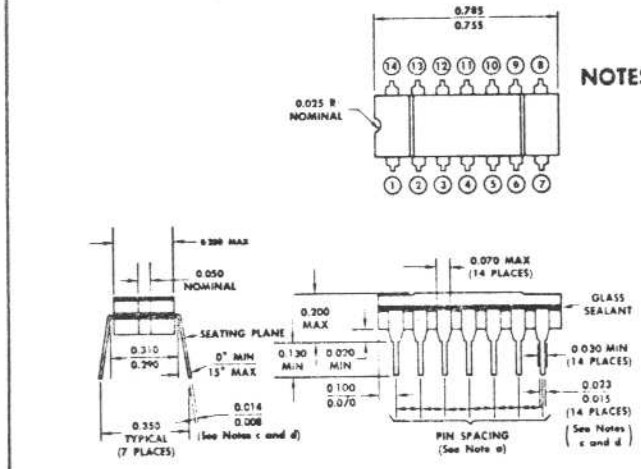
3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 4.

4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7440N
Sprague Part No. USN7440A
National Semi-conductor Corp. Part No. DM8040N
Motorola Part No. MC7440P

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

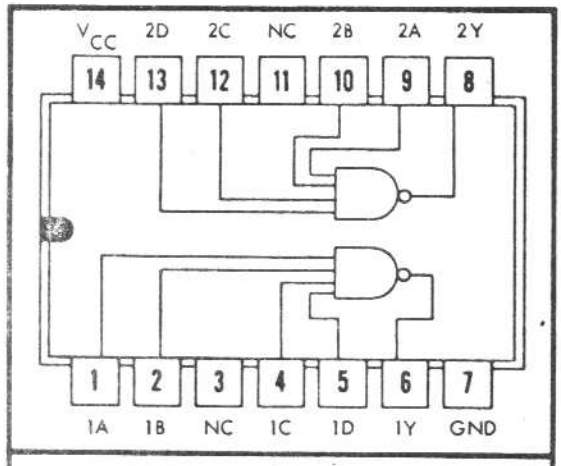
d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

SN7440N

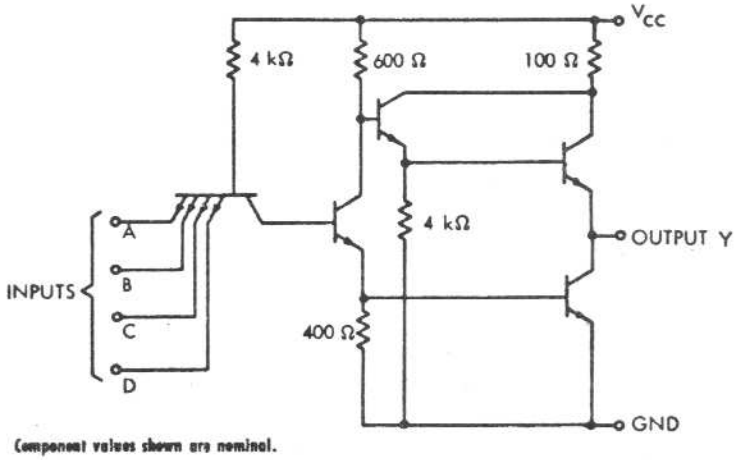
DUAL 4-INPUT POSITIVE NAND BUFFER



positive logic

$Y = \overline{ABCD}$

schematic (each gate)



(component values shown are nominal.)

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Output, N . . . . . 1 to 30

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1	$V_{CC} = 4.75$ V, $V_{out(0)} \leq 0.4$ V	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2	$V_{CC} = 4.75$ V, $V_{out(1)} \geq 2.4$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	$V_{CC} = 4.75$ V, $V_{in} = 0.8$ V, $I_{load} = -1.2$ mA	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	1	$V_{CC} = 4.75$ V, $V_{in} = 2$ V, $I_{sink} = 48$ mA		0.28‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	5	$V_{CC} = 5.25$ V	−18		−70	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	$V_{CC} = 5$ V, $V_{in} = 5$ V		8.6‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	$V_{CC} = 5$ V, $V_{in} = 0$		2‡		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 30$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	$C_l = 15$ pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	$C_l = 15$ pF		18	29	ns

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			
	B	ECN NO. 3972	P.S	27AUG	[illegible]

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
DUAL 2-WIDE 2-INPUT E/OR-INVERT GATES
V3008EN - WITH EXPANDER INPUTS (SN7450N)
V3008EP - NO EXPANDER INPUTS (SN7451N)

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 4

4. MANUFACTURER'S NAME AND PART NO.

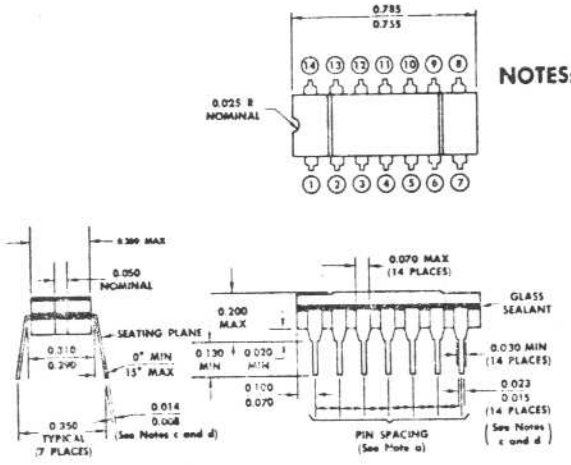
Texas Instrument, Part No. SN7450N/SN7451N
Sprague Part No. USN7450A/USN7451A
Motorola Part No. MC7450P/MC7451P

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.		THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
REMOVE BURRS & SHARP EDGES	DRAFTSMAN B Weller	DATE 3/24/67	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7450/SN7451N
DIMENSIONS ARE IN INCHES	DESIGNER		
PLATING APPLY AFTER PLATING	CHECKER F Weller	3/24/67	
TOLERANCES ON FRACTIONS: ± 1/64 DECIMALS: ± .005 ANGLES: ± 1/2°	ENGINEER [illegible]	3/24/67	SIZE A | SYMBOL | DRAWING NO. V3008EN/EP | REV B
MATERIAL: N/A	RELEASES		
FINISH: N/A	LOCAL RELEASE		SCALE: NONE | SHEET 1 OF 4

FORM 5033A (8/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

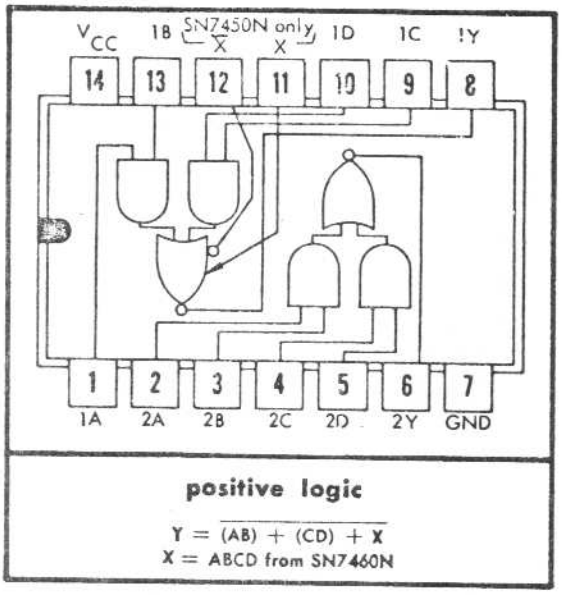
c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

SN7450N/SN7451N
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES



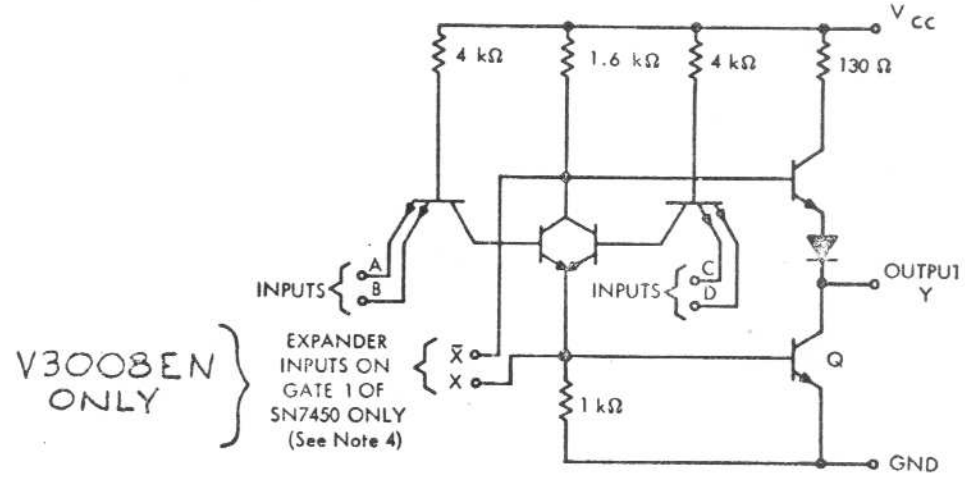
positive logic

$Y = \overline{(AB) + (CD) + X}$

$X = ABCD$ from SN7460N

NOTE: Expander nodes X and $\overline{X}$ are on the SN7450N only. Make no external connection to pins (11) and (12) of the SN7451N.

schematic (each gate)



NOTES: 1. Component values shown are nominal.
2. Both SN7450 expander inputs are used simultaneously for expanding with the SN7460.
3. If expander is not used leave pins (1) and (2) open.
4. Make no external connection to pins (1) and (2) of the SN7451.
5. A total of four expander gates may be connected to the SN7450 expander.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . . 1 to 10

electrical characteristics, $T_A = 0°C$ to 70°C, pins (1) and (2) open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	7	$V_{CC} = 4.75$ V, $V_{out(0)} \leq 0.4$ V	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	8	$V_{CC} = 4.75$ V, $V_{out(1)} \geq 2.4$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	8	$V_{CC} = 4.75$ V, $V_{in} = 0.8$ V, $I_{load} = -400\ \mu A$	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	7	$V_{CC} = 4.75$ V, $V_{in} = 2$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	9	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	10	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	11	$V_{CC} = 5.25$ V	−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current (each gate)	12	$V_{CC} = 5$ V, $V_{in} = 5$ V		3.7‡		mA
$I_{CC(1)}$	Logical 1 level supply current (each gate)	13	$V_{CC} = 5$ V, $V_{in} = 0$		2‡		mA

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

electrical characteristics (SN7450 only) using expander inputs, $T_A = 0°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_X	Expander current	14	$V_{CC} = 4.75$ V, $V_1 = 0.4$ V, $I_{sink} = 16$ mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	15	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA, $I_1 = 0.62$ mA, $R_1 = 0$			1	V
$V_{out(1)}$	Logical 1 output voltage	16	$V_{CC} = 4.75$ V, $I_{load} = -400\ \mu A$, $I_1 = 270\ \mu A$, $I_2 = -270\ \mu A$	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	15	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA, $I_1 = 0.43$ mA, $R_1 = 130\ \Omega$		0.22‡	0.4	V

‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, pins (1) and (2) open, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	$C_1 = 15$ pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	$C_1 = 15$ pF		18	29	ns

FIRST USED ON					
	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			
	B	CHG PER ECN NO. 3246	J.D	5/70	
	C	ECN # 3403	R.B.	9/70	

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Quad 2 and/or invert gate with expander inputs.
V3008ER - with expander inputs (SN7453N)
V3008ES - no expander inputs (SN7454N)

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 4

4. MANUFACTURER'S NAME AND PART NO.

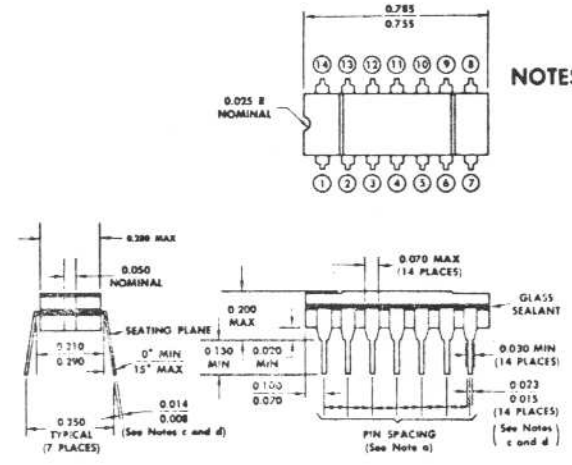
Texas Instrument, Part No. SN7453N/SN7454N
Sprague Part No. US 7453A/US 7454A
Motorola Part No. MC7453P/MC7454P

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED REMOVE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES DIMENSIONS APPLY AFTER PLATING	WORK AUTH NO.		FOXBORO — THE FOXBORO COMPANY, FOXBORO, MASSACHUSETTS, U.S.A.			
TOLERANCES ON FRACTIONS: ± 1/64 DECIMALS: ± .005 ANGLES: ± 1/2°	DRAFTSMAN B. Wallen	DATE	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7453N/SN7454N			
	DESIGNER					
	CHECKER B. Wallen	3/24/69				
MATERIAL: N/A	ENGINEER	3/24/69	SIZE A	SYMBOL	DRAWING NO. V3008ER/ES	REV C
FINISH: N/A	RELEASED					
	LOCAL RELEASE		SCALE: NONE		SHEET 1 OF 4	

FORM 6083A (6/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

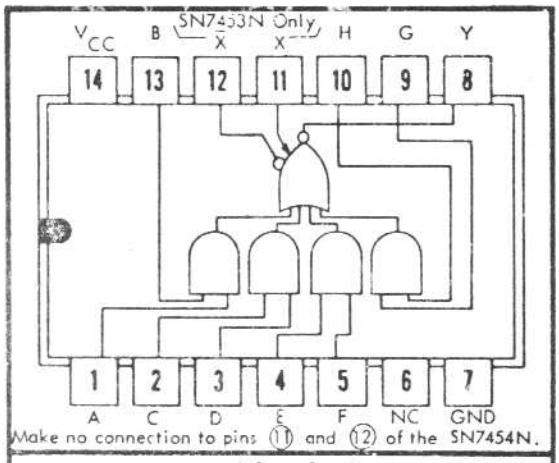
c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

SN7453N, SN7454N
4-WIDE 2-INPUT AND-OR-INVERT GATES



positive logic

$$Y = \overline{(AB) + (CD) + (EF) + (GH) + X}$$

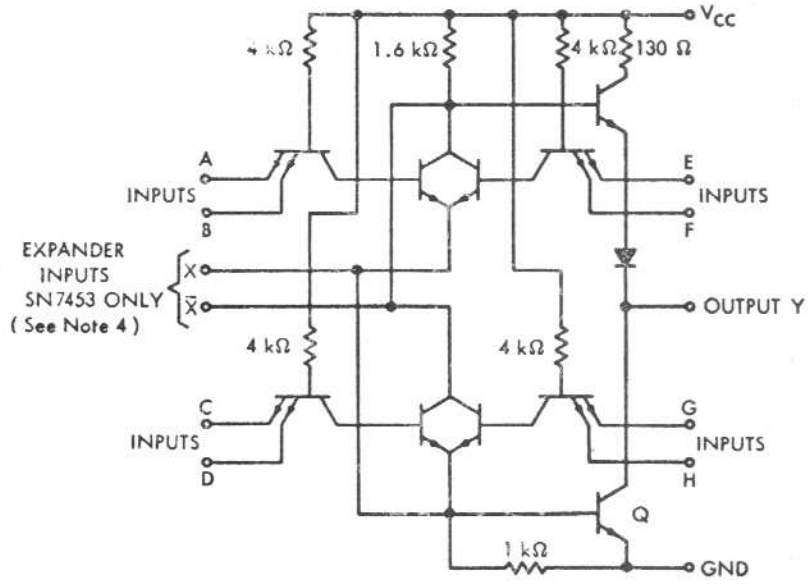
$$X = ABCD \text{ from SN7460N}$$

NOTE: Expander nodes X and $\bar{X}$ are on the SN7453N only.

NC — No internal connection.
†Patented by Texas Instruments

(V3008ER)

schematic



NOTES:
1. Component values shown are nominal.
2. Both SN7453 expander inputs are used simultaneously for expanding with the SN7460.
3. If SN7453 expander is not used leave pins (1) and (2) open.
4. Make no external connection to pins (1) and (2) of the SN7454.
5. A total of four expander gates may be connected to the SN7453 expander inputs.

electrical characteristics, $T_A = 0°C$ to 70°C, pins (1) and (2) open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	7	$V_{CC} = 4.75$ V, $V_{out(0)} \leq 0.4$ V	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	8	$V_{CC} = 4.75$ V, $V_{out(1)} \geq 2.4$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	8	$V_{CC} = 4.75$ V, $V_{in} = 0.8$ V, $I_{load} = -400\ \mu A$	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	7	$V_{CC} = 4.75$ V, $V_{in} = 2$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	9	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	10	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	11	$V_{CC} = 5.25$ V	−18		−55	mA
$I_{CC(0)}$	Logical 0 level supply current	12	$V_{CC} = 5$ V, $V_{in} = 5$ V		3.7 ‡		mA
$I_{CC(1)}$	Logical 1 level supply current	13	$V_{CC} = 5$ V, $V_{in} = 0$		2 ‡		mA

†Not more than one output should be shorted at a time.

‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

electrical characteristics (SN7453 only) using expander inputs, $T_A = 0°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_X	Expander current	14	$V_{CC} = 4.75$ V, $V_I = 0.4$ V, $I_{sink} = 16$ mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	15	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA, $I_1 = 0.62$ mA, $R_1 = 0$			1	V
$V_{out(1)}$	Logical 1 output voltage	16	$V_{CC} = 4.75$ V, $I_{load} = -400\ \mu A$, $I_1 = 270\ \mu A$, $I_2 = -270\ \mu A$	2.4	3.3‡		V
$V_{out(0)}$	Logical 0 output voltage	15	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA, $I_1 = 0.43$ mA, $R_1 = 130\ \Omega$		0.22‡	0.4	V

‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics (SN7453 and SN7454), $V_{CC} = 5$ V, $T_A = 25°C$, pins (1) and (2) open, $N = 10$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	50	$C_1 = 15$ pF		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	50	$C_1 = 15$ pF		18	29	ns

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Dual 4-Input Expander

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 4

4. MANUFACTURER'S NAME AND PART NO.

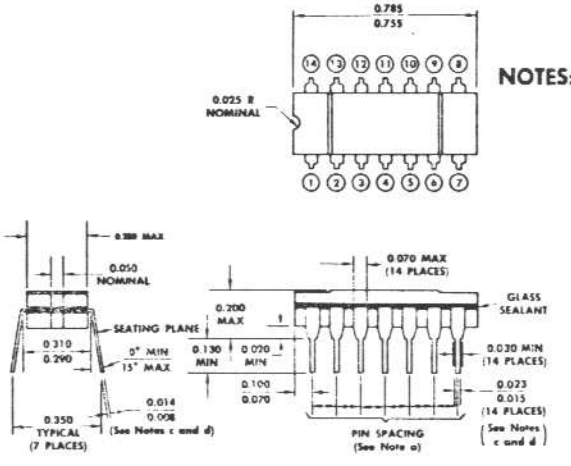
Texas Instrument, Part No. SN7460N
Sprague Part No. USN7460A
Motorola Part No. MC7460P

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

LESS OTHERWISE SPECIFIED SHARP EDGES DIMENSIONS ARE IN INCHES FINISH APPLY AFTER PLATING TOLERANCES ON FRACTIONS ± 1/64 DECIMALS ± .005 ANGLES ± 1/2° MATERIAL: N/A FINISH: N/A	WORK AUTH NO.		THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
	DRAFTSMAN B Walker	DATE 3/24/70	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7460N
	DESIGNER		
	CHECKER B Walker	3/24/70	
	ENGINEER S.P. Desa	3/24/70	SIZE A | SYMBOL | DRAWING NO. V3008ET | REV A
	RELEASED		
	LOCAL RELEASE		SCALE: NONE | SHEET 1 OF 4

5083A (6/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

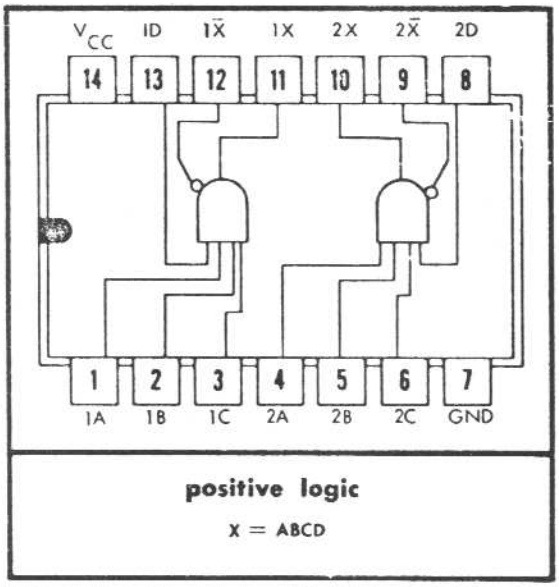
c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

SN7460N
DUAL 4-INPUT EXPANDER

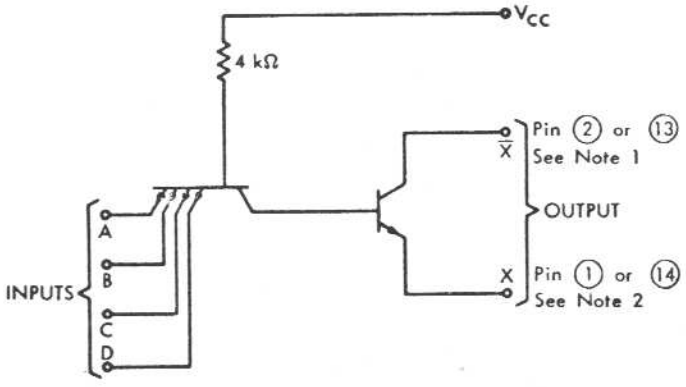


positive logic

X = ABCD

NOTE: Connect pin (9) or (12) to pin (12) of SN7450N or SN7453N.
Connect pin (10) or (11) to pin (11) of SN7450N or SN7453N.

schematic



NOTES: 1. Connect pin (2) or (13) to pin (2) of SN7450 or SN7453.
2. Connect pin (1) or (14) to pin (1) of SN7450 or SN7453.
3. Component values shown are nominal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V

Maximum number of expanders that may be fanned-in to one SN7450 or one SN7453 4

electrical characteristics (unless otherwise noted $T_A = 0°C$ to $70°C$)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure output on level	17	$V_{CC} = 4.75$ V, $V_1 = 1$ V, $R = 1.1$ kΩ, $T_A = 0°C$	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure output off level current	18	$V_{CC} = 4.75$ V, $V_1 = 4.5$ V, $R = 1.2$ kΩ, $I_{off} = 0.15$ mA, $T_A = 0°C$			0.8	V
V_{on}	Output voltage on level	17	$V_{CC} = 4.75$ V, $V_{in} = 2$ V, $V_1 = 1$ V, $R = 1.1$ kΩ, $T_A = 0°C$			0.4	V
I_{off}	Output off level current	18	$V_{CC} = 4.75$ V, $V_{in} = 0.8$ V, $V_1 = 4.5$ V, $R = 1.2$ kΩ, $T_A = 0°C$			270	μA
I_{on}	Output on level current	19	$V_{CC} = 4.75$ V, $V_{in} = 2$ V, $V_1 = 1$ V	−0.43			mA
$I_{in(0)}$	Logical 0 level input current (each input)	18	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	20	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
$I_{CC(on)}$	On level supply current (each gate)	21	$V_{CC} = 5$ V, $V_{in} = 5$ V, $V_1 = 0.85$ V, $T_A = 25°C$		0.6		mA
$I_{CC(off)}$	Off level supply current (each gate)	21	$V_{CC} = 5$ V, $V_{in} = 0$, $V_1 = 0.85$ V, $T_A = 25°C$		1		mA

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level (through SN7450 or SN7453)	51	$C_1 = 15$ pF		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level (through SN7450 or SN7453)	51	$C_1 = 15$ pF		20	34	ns

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			
	B	ECN # 3403	K.B.		

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Single-Phase J-K Flip-Flop

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5

4. MANUFACTURER'S NAME AND PART NO.

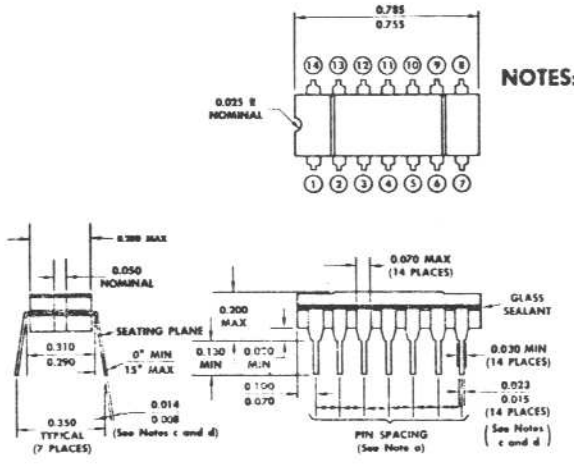
Texas Instrument, Part No. SN7470N
Sprague Part No. US 7470A

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.	FOXBORO	THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
REMOVE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES TOLERANCES APPLY AFTER PLATING	DRAFTSMAN P. Walker 3/24/70		
	DESIGNER	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7470N	
TOLERANCES ON FRACTIONS: ± 1/64 DECIMALS: ± .005 ANGLES: ± 1/2°	CHECKER B. Walker 3/24/70		
MATERIAL: N/A	ENGR. P. Walker 3/24/70	SIZE A	SYMBOL
FINISH: N/A	RELEASED	DRAWING NO. V3008EW	REV B
	LOCAL RELEASE	SCALE: NONE	SHEET 1 OF 5

J 5083A (8/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

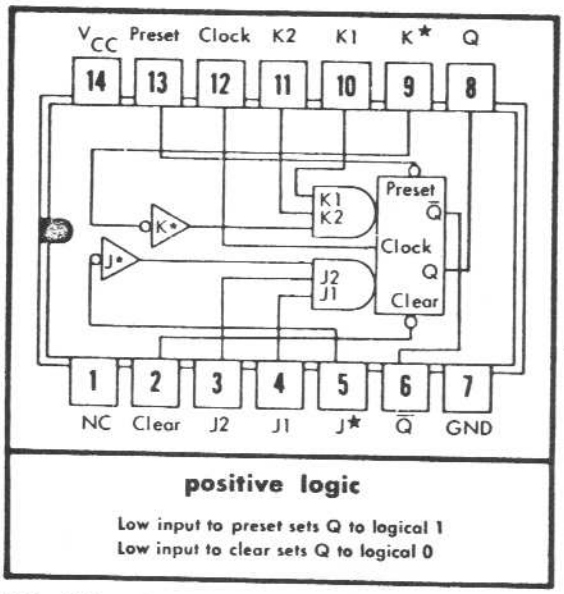
c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

SN7470N
J-K FLIP-FLOP



positive logic

Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0

NOTE: Clock must be at logical 0 prior to the application of preset or clear functions.

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. $J = J1 \cdot J2 \cdot \overline{J★}$
2. $K = K1 \cdot K2 \cdot \overline{K★}$
3. t_n = bit time before clock pulse.
4. t_{n+1} = bit time after clock pulse.
5. If inputs J★ or K★ are not used they must be grounded.

description

The SN7470 is a monolithic, edge-triggered J-K flip-flop featuring gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

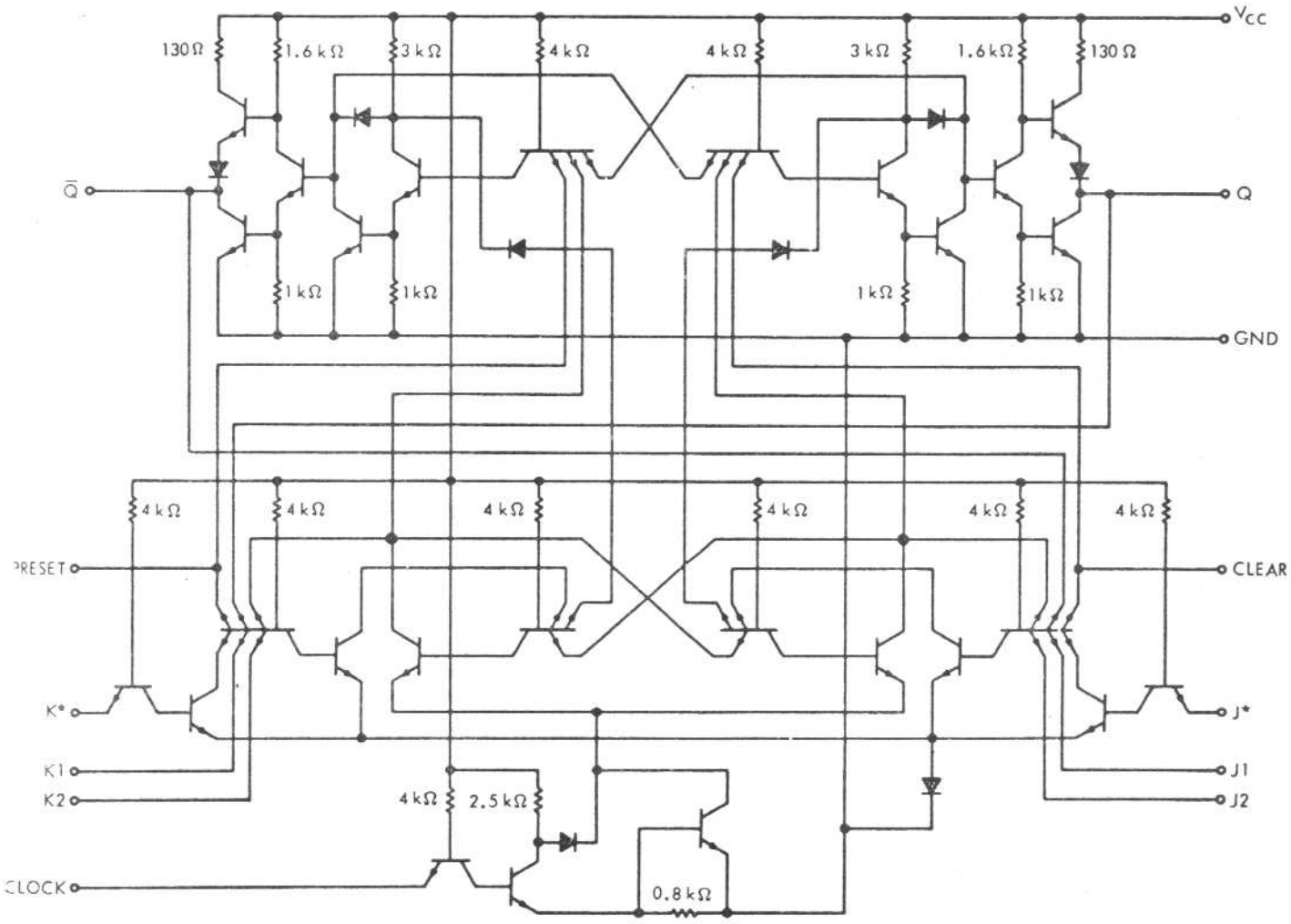
Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse; and after the clock input threshold voltage has been passed, the gated inputs are locked out.

The SN7470 flip-flop is ideally suited for medium-and high-speed applications, and can be used for a significant saving in system power dissipation and package count where input gating is required.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . . 1 to 10
Clock Pulse Transition Time to Logical 1 Level, $t_{1(clock)}$ (See Figure 53) . . . . . 5 to 150 ns
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 53) . . . . . $\geq$ 20 ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 52) . . . . . $\geq$ 25 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 52) . . . . . $\geq$ 25 ns

schematic



Component values shown are nominal.

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	22	$V_{CC} = 4.75$ V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	23	$V_{CC} = 4.75$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	22	$V_{CC} = 4.75$ V, $I_{load} = -400\ \mu A$	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	23	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J★, K1, K2, K★, or clock	24	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	24	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J★, K1, K2, K★, or clock	25	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	25	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			80	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	26	$V_{CC} = 5.25$ V, $V_{in} = 0$	−18		−57	mA
I_{CC}	Supply current	25	$V_{CC} = 5$ V, $V_{in} = 5$ V		13‡		mA

†Not more than one output should be shorted at a time.

‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	53	$C_L = 15$ pF	20	35		MHz
t_{setup}	Minimum input setup time	53	$C_L = 15$ pF		10	20	ns
t_{hold}	Minimum input hold time	53	$C_L = 15$ pF		0	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	52	$C_L = 15$ pF			50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	52	$C_L = 15$ pF			50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	53	$C_L = 15$ pF	10	27	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	53	$C_L = 15$ pF	10	18	50	ns

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Single Master/Slave Flip-Flop

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5

4. MANUFACTURER'S NAME AND PART NO.

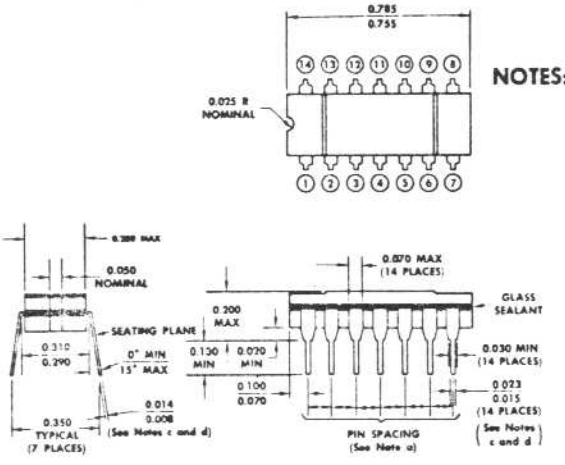
Texas Instrument, Part No. SN7472N
Sprague Part No. USN7472A
Motorola Part No. MC7472P

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

ESS OTHERWISE SPECIFIED	WORK AUTH NO.		THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
VE BURRS & SHARP EDGES TIONS ARE IN INCHES NGS APPLY AFTER PLATING	DRAFTSMAN	DATE	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7472N
ANCES ON IONS ± 1/64 ALS ± .005 ES ± 1/2°	DESIGNER CHECKED		
TERIAL:	ENGR		SIZE A | SYMBOL | DRAWING NO. V300SEX | REV A
NISH:	RELEASED		SCALE: NONE | SHEET 1 OF 5
	LOCAL RELEASE		

FORM 5033A (6/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

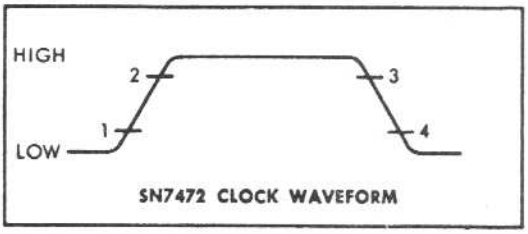
e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

description

The SN7472 J-K flip-flop is based on the master-slave principle. This device has AND gate inputs for entry into the master section which are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND gate inputs
4. Transfer information from master to slave.

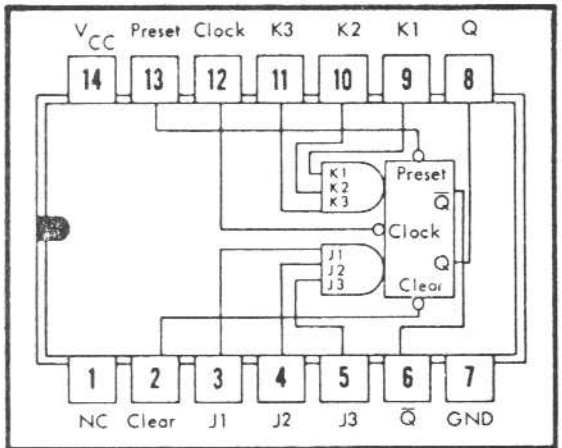


SN7472 CLOCK WAVEFORM

recommended operating conditions

Supply Voltage V_{CC}	4.75 V to 5.25 V
Fan-Out From Each Output, N	1 to 10
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 54)	$\geq$ 20 ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 55)	$\geq$ 25 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 55)	$\geq$ 25 ns
Input Setup Time, t_{setup} (See Figure 54)	$\geq$ Applied Clock Pulse Width
Input Hold Time, t_{hold}	$\geq$ 0

SN7472N
J-K MASTER-SLAVE FLIP-FLOP



positive logic

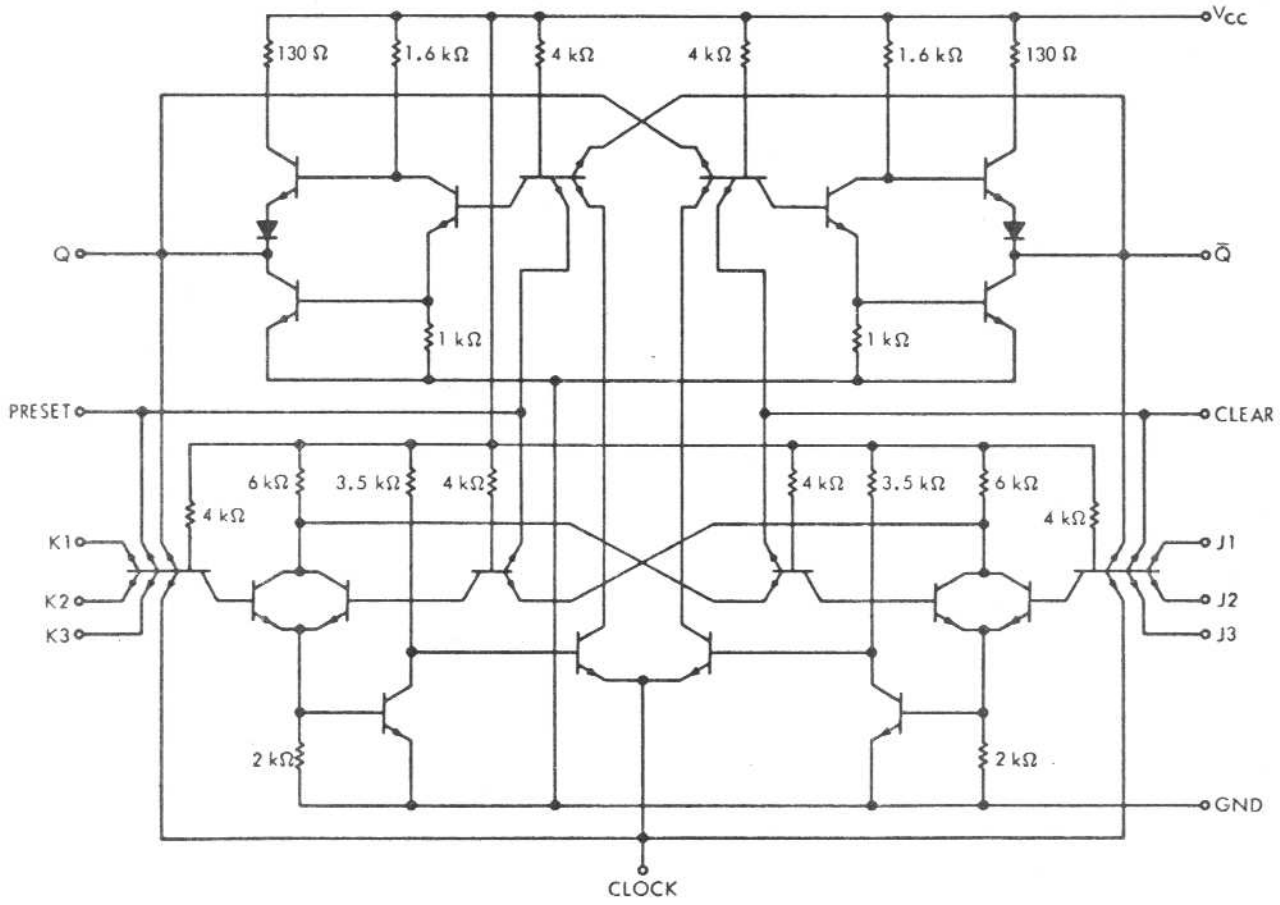
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. $J = J1 \cdot J2 \cdot J3$
2. $K = K1 \cdot K2 \cdot K3$
3. t_n = bit time before clock pulse.
4. t_{n+1} = bit time after clock pulse.

NC — No internal connection.
†Patented by Texas Instruments

schematic



Component values shown are nominal.

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	27	$V_{CC} = 4.75$ V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	27	$V_{CC} = 4.75$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	27	$V_{CC} = 4.75$ V, $I_{load} = -400\ \mu A$	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	28	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	29	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	29	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	30	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset, clear, or clock	30	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			80	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	31	$V_{CC} = 5.25$ V, $V_{in} = 0$	−18		−57	mA
I_{CC}	Supply current	30	$V_{CC} = 5$ V, $V_{in} = 5$ V		8‡		mA

†Not more than one output should be shorted at a time.

‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	54	$C_1 = 15$ pF	10	15		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	55	$C_1 = 15$ pF		26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	55	$C_1 = 15$ pF		34	50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	54	$C_1 = 15$ pF	10	26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	54	$C_1 = 15$ pF	10	34	50	ns

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1512			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Dual Master/Slave Flip-Flop

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5

4. MANUFACTURER'S NAME AND PART NO.

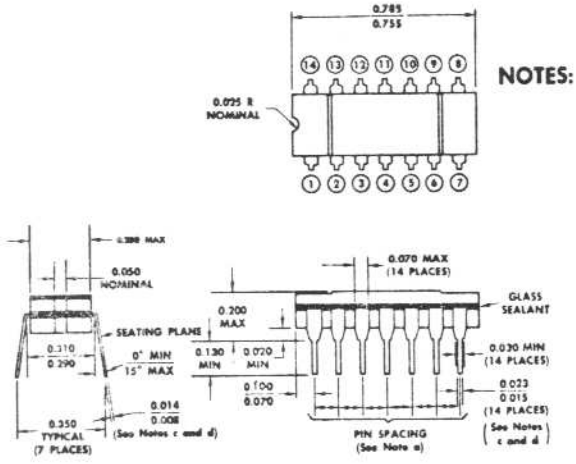
Texas Instrument, Part No. SN7473N
Sprague Part No. USN7473A
National Semiconductor Corp. Part No. DM8501N
Motorola Part No. MC7473P

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

ESS OTHERWISE SPECIFIED	WORK AUTH NO.	FOXBORO	THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
VE BURRS & SHARP EDGES	DRAFTSMAN [illegible] DATE 2/24/69		
NSIONS ARE IN INCHES	DESIGNER	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN74 73N	
DINGS APPLY AFTER PLATING	CHECKER [illegible] 2/24/69		
ERANCES ON CTIONS: ± 1/64 MALS: ± .003 LES: ± 1/2°	ENGR [illegible] 3/24/69	SIZE A	SYMBOL
TERIAL: N/A	RELEASED	DRAWING NO. V3008EY	REV A
NISH: N/A	LOCAL RELEASE	SCALE: NONE	SHEET 1 OF 5

FORM 6083A (8/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

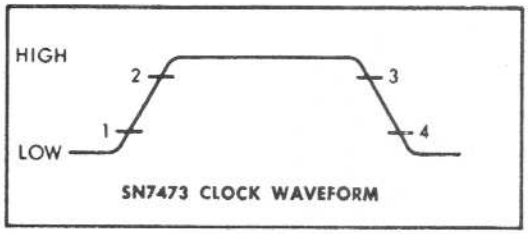
e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

description

The SN7473 J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

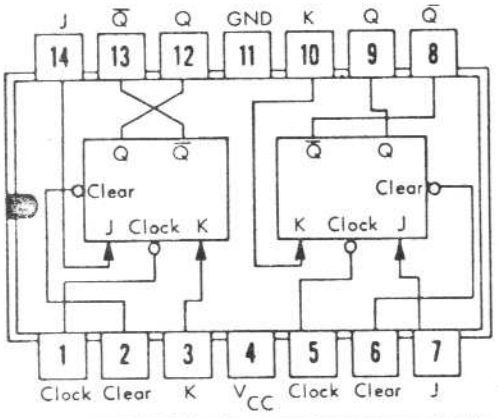


SN7473 CLOCK WAVEFORM

recommended operating conditions

Supply Voltage V_{CC}	4.75 V to 5.25 V
Fan-Out From Each Output, N	1 to 10
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 54)	$\geq$ 20 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 55)	$\geq$ 25 ns
Input Setup Time, t_{setup} (See Figure 54)	$\geq$ Applied Clock Pulse Width
Input Hold Time, t_{hold}	$\geq$ 0

SN7473N
DUAL J-K MASTER-SLAVE FLIP-FLOP



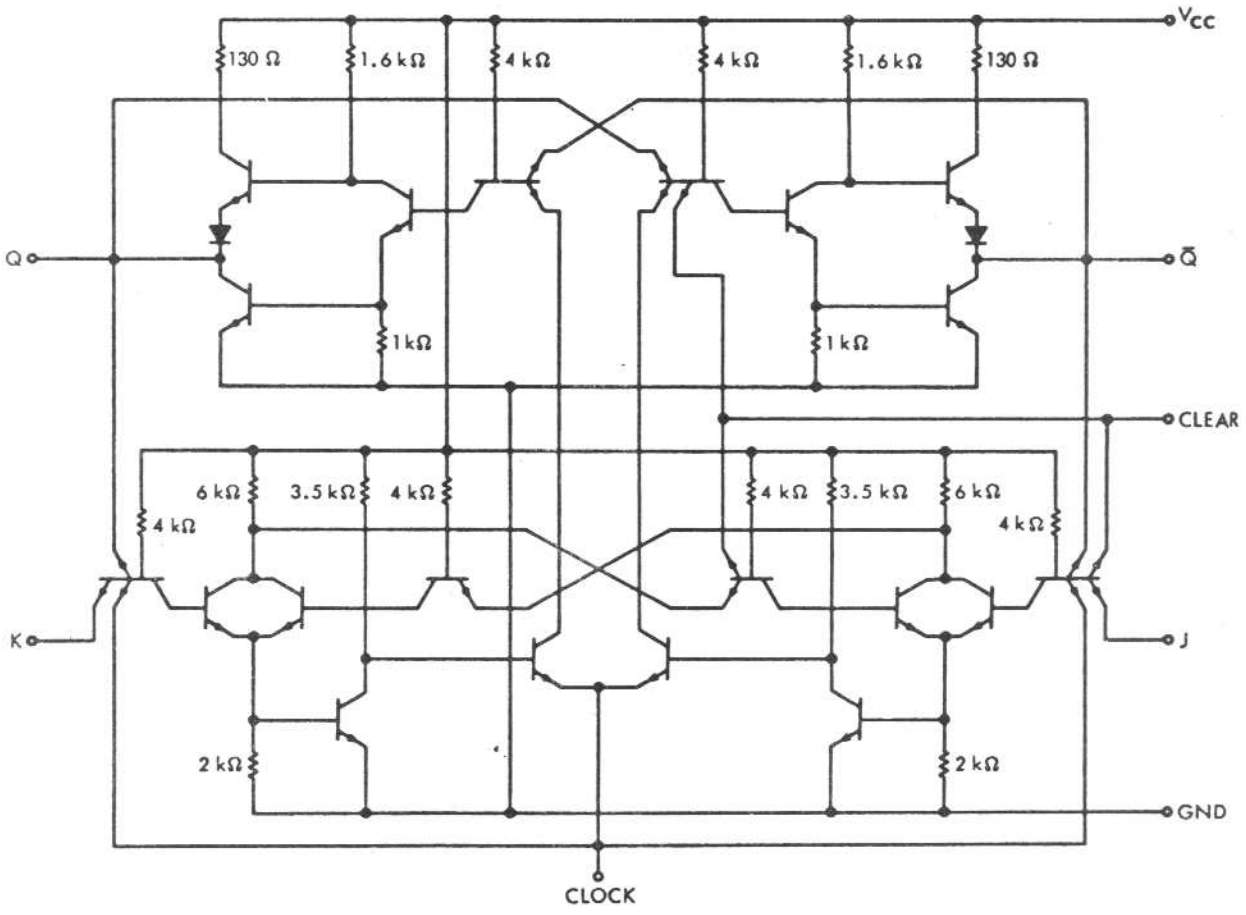
positive logic

Low input to clear sets Q to logical 0 regardless of clock state.

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

schematic (each flip-flop)



Component values shown are nominal.

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	32	$V_{CC} = 4.75$ V		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	32	$V_{CC} = 4.75$ V				0.8	V
$V_{out(1)}$	Logical 1 output voltage	32	$V_{CC} = 4.75$ V,	$I_{load} = -400\ \mu A$	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	33	$V_{CC} = 4.75$ V,	$I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	34	$V_{CC} = 5.25$ V,	$V_{in} = 0.4$ V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	34	$V_{CC} = 5.25$ V,	$V_{in} = 0.4$ V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	35	$V_{CC} = 5.25$ V,	$V_{in} = 2.4$ V			40	μA
			$V_{CC} = 5.25$ V,	$V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear or clock	35	$V_{CC} = 5.25$ V,	$V_{in} = 2.4$ V			80	μA
			$V_{CC} = 5.25$ V,	$V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	36	$V_{CC} = 5.25$ V,	$V_{in} = 0$	−18		−57	mA
I_{CC}	Supply current (each flip-flop)	35	$V_{CC} = 5$ V,	$V_{in} = 5$ V		8‡		mA

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, $N = 10$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	54	$C_1 = 15$ pF	10	15		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	55	$C_1 = 15$ pF		26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	55	$C_1 = 15$ pF		34	50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	54	$C_1 = 15$ pF	10	26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	54	$C_1 = 15$ pF	10	34	50	ns

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN 1912			

REV STATUS OF SHEETS	REV	A	A	A	A	A	A										
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
DRAFTING	B. WALKER	B. WALKER	7-20-68
DESIGNED			

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT, INTEGRATED
DUAL IN-LINE PACKAGE
TYPE SN7474N

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED J. P. DENSLER	7/24/69	
LOCAL RELEASE M. J. COOK	5/11/69	
CORPORATE RELEASE FRANKLIN	JUN 73	

SIZE A | B | DRAWING NUMBER V3008E7

DESIGNED FOR | SCALE | WT | SHEET 1 OF 6

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Dual "D" Type Flip Flop

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 6.

4. MANUFACTURER's NAME AND PART NO.

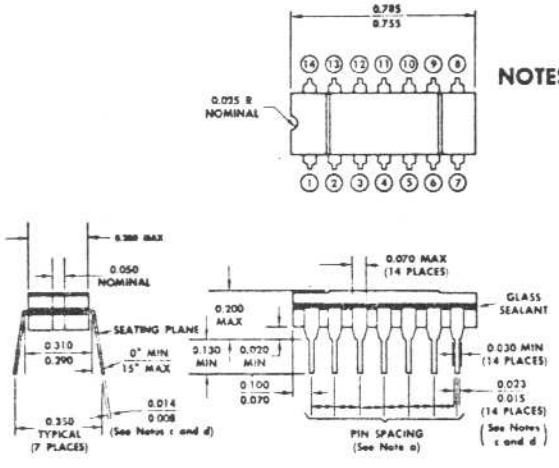
Texas Instrument, Part No. SN7474N
Sprague Part No. USN7474A
National Semiconductor Corp. Part No. DM8510N

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	V30083E7	A
		SCALE:	SHEET 1 OF

DO NOT SCALE PRINT

FORM A816-088-4/66



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

description

The SN7474 is a monolithic, dual, D-type, edge-triggered flip-flop featuring direct clear and preset inputs and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the Q output on the positive edge of the clock pulse.

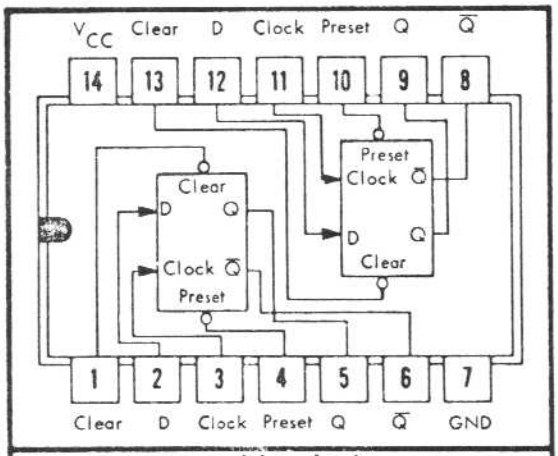
Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed the data input (D) is locked out.

The SN7474 dual flip-flop has the same clocking characteristics as the SN7470 gated (edge-triggered) flip-flop and both are ideally suited for medium- and high-speed applications. The SN7474 can be used at a significant saving in system power dissipation and package count in applications where input gating is not required.

recommended operating conditions

Supply Voltage V_{CC}	4.75 V to 5.25 V
Fan-Out From Each Output, N	1 to 10
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 56)	$\geq$ 30 ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 53)	$\geq$ 30 ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 53)	$\geq$ 30 ns

SN7474N
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOP



positive logic

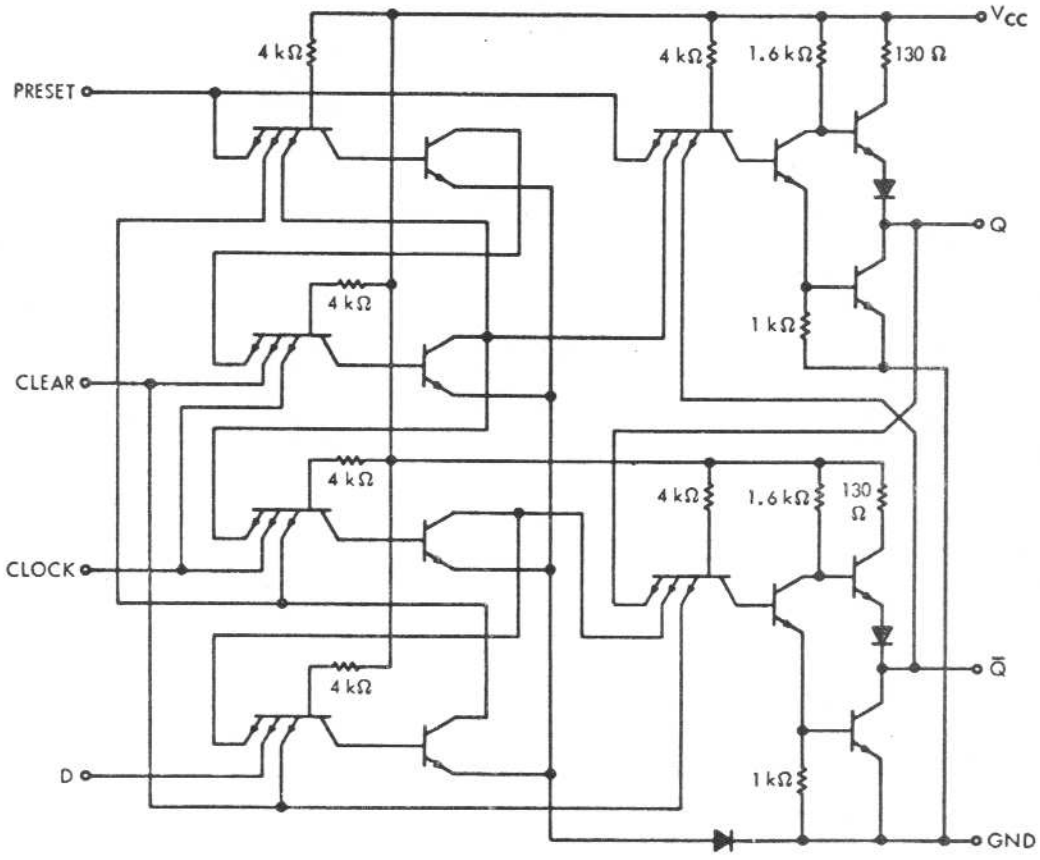
a. Low input to clear sets Q to logical 0.
b. Low input to preset sets Q to logical 1.
c. Clear or preset inputs dominate regardless of clock and D inputs

TRUTH TABLE (Each Flip-Flop)

t_n	t_{n+1}	
INPUT D	OUTPUT Q	OUTPUT $\overline{Q}$
0	0	1
1	1	0

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

schematic (each flip-flop)



Component values shown are nominal.

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	37	$V_{CC} = 4.75$ V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	37	$V_{CC} = 4.75$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	37	$V_{CC} = 4.75$ V, $I_{load} = -400\ \mu A$	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	38	$V_{CC} = 4.75$ V, $I_{sink} = 16$ mA		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	39	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	39	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	40	$V_{CC} = 5.25$ V, $V_{in} = 4.5$ V			40	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	40	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			80	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	40	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			120	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current†	41	$V_{CC} = 5.25$ V, $V_{in} = 0$	−18		−57	mA
I_{CC}	Supply current (each flip-flop)	40	$V_{CC} = 5$ V, $V_{in} = 5$ V		8.5‡		mA

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	56	$C_1 = 15$ pF	15	25		MHz
t_{setup}	Minimum input setup time	56	$C_1 = 15$ pF		15	20	ns
t_{hold}	Minimum input hold time	56	$C_1 = 15$ pF		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	52	$C_1 = 15$ pF			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	52	$C_1 = 15$ pF			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	56	$C_1 = 15$ pF	10	20	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	56	$C_1 = 15$ pF	10	28	50	ns

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN 1912			

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A						
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

DRAWN E.V/ALEE	CHK'D [illegible]	DATE 5/24/67
DRAFTING		
DESIGNED		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT, INTEGRATED
DUAL IN-LINE PACKAGE
TYPE SN7475N

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

APPROVED J. DEWLER	5/24/67	
LOCAL RELEASE M. COOK	7/11/67	
CORPORATE RELEASE V. FRANKLIN	JUN 73	

SIZE A | B

DRAWING NUMBER V3008FA

DESIGNED FOR

SCALE | WT | SHEET 1 OF 10

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Quadruple Latch

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

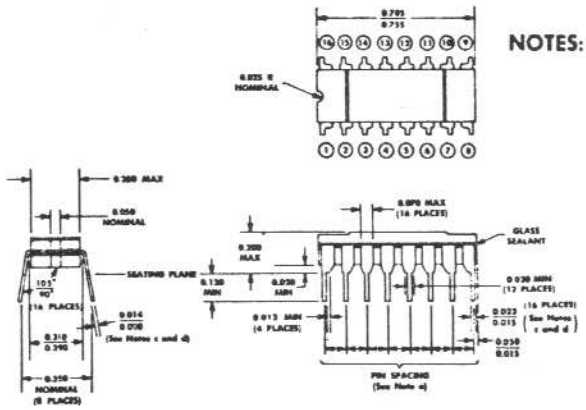
3.1 See Sheets 6, 7, 8, 9, & 10.

4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7475N
Sprague Part No. USN7475B
National Semiconductor Corp. Part No. DM855ON
Motorola Part No. MC7475P

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	V3008FA	A
DO NOT SCALE PRINT	SCALE:	SHEET 2 OF	



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (1) and (16)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

16-PIN FUNCTIONS

THE FOXBORO COMPANY SYSTEMS DIVISION	B V3008 FA
	Sheet 3 of

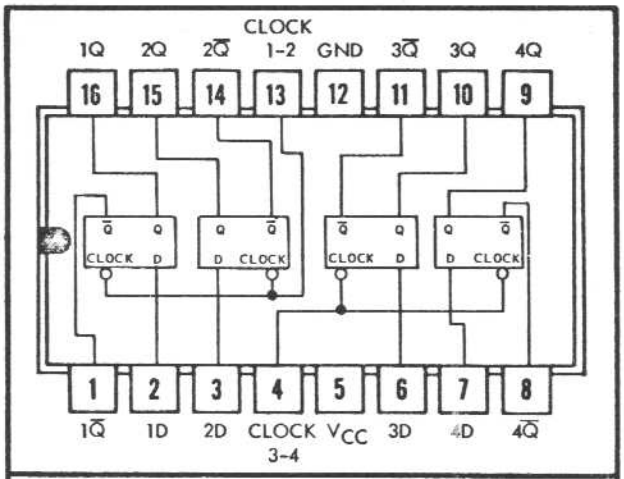
Rev. A

Form 5039 (6/68)

logic

TRUTH TABLE (Each Latch)		
t_n	t_{n+1}	
D	Q	$\overline{Q}$
1	1	0
0	0	1

NOTES: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.



positive logic

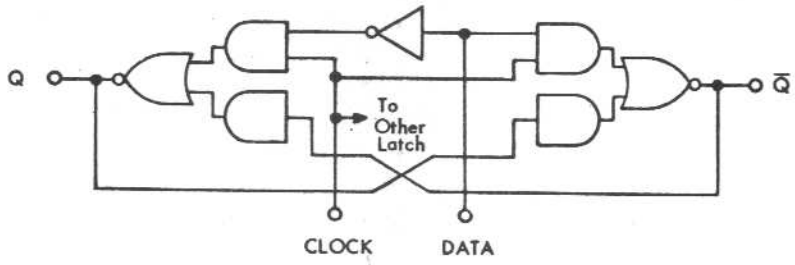
See Truth Table

description

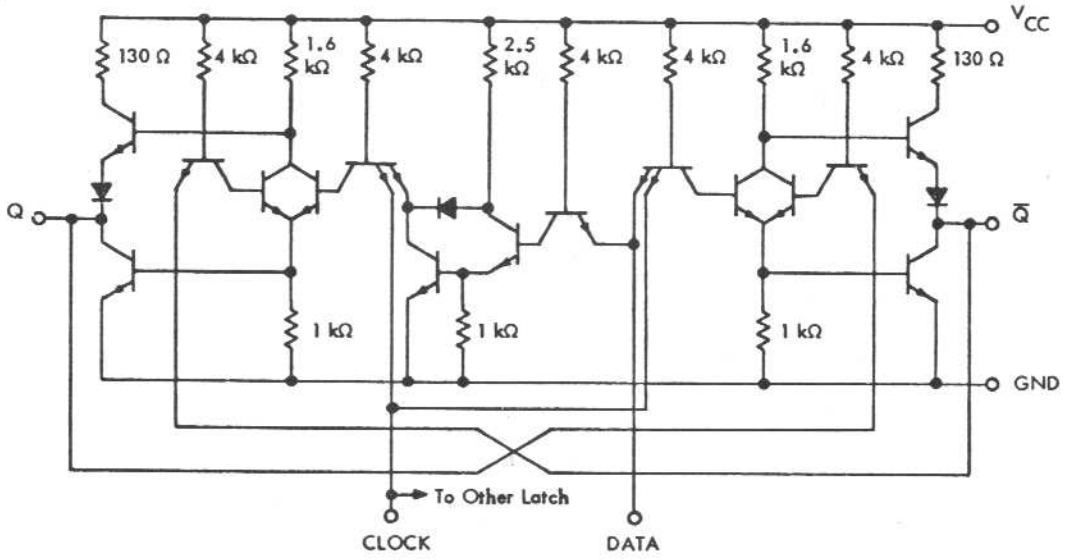
The SN7475N is a monolithic, quadruple, bistable latch with complementary Q and $\overline{Q}$ outputs. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high. Pin assignments, or physical placement of the logical functions, were selected to coincide with the physical placement of logical functions of other Series 74 circuits which are most likely to be used as inputs to, or outputs from, the SN7475N.

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Applications are shown for the SN7475N being used for temporary storage of 4-bit binary data and as a dual master-slave flip-flop with two-phase clocking.

functional block diagram (each latch)



schematic (each latch)



recommended operating conditions

Supply Voltage V_{CC} (See Note 1) . . . . . 4.75 V to 5.25 V

Fan-Out From Outputs . . . . . 1 to 10

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V

Input Voltage V_{in} (See Notes 1 and 2) . . . . . 5.5 V

Operating Free-Air Temperature Range . . . . . 0°C to 70°C

Storage Temperature Range . . . . . -55°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics, T_A = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	1	V_{CC}=4.75 V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	2	V_{CC}=4.75 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 and 2	V_{CC}=4.75 V, I_{load}= -400 µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1 and 2	V_{CC}=4.75 V, I_{sink}=16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at D	3	V_{CC}=5.25 V, V_{in}=0.4 V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	3	V_{CC}=5.25 V, V_{in}=0.4 V			-6.4	mA
$I_{in(1)}$	Logical 1 level input current at D	3	V_{CC}=5.25 V, V_{in}=2.4 V			80	µA
			V_{CC}=5.25 V, V_{in}=5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	3	V_{CC}=5.25 V, V_{in}=2.4 V			160	µA
			V_{CC}=5.25 V, V_{in}=5.5 V			1	mA
I_{OS}	Short-circuit output current†	4	V_{CC}=5.25 V, V_{out}=0	-18		-57	mA
I_{CC}	Supply current	5	V_{CC}=5 V, T_A=25°C		32		mA

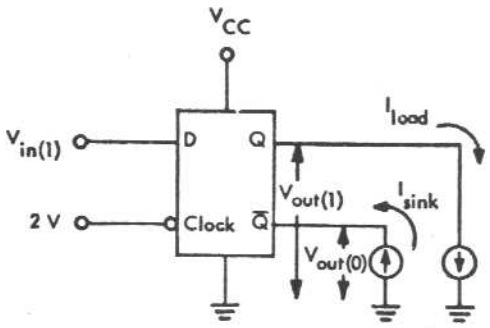
† Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	5A	C_L = 15 pF, R_L = 400 Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	5A	C_L = 15 pF, R_L = 400 Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	5A	C_L = 15 pF, R_L = 400 Ω	0	15†		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	5A	C_L = 15 pF, R_L = 400 Ω	0	6†		ns
$t_{pd1(D-Q)}$	Propagation delay time from D input to Q output	5A	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(D-Q)}$	Propagation delay time from D input to Q output	5A	C_L = 15 pF, R_L = 400 Ω		14	25	ns
$t_{pd1(D-\overline{Q})}$	Propagation delay time from D input to $\overline{Q}$ output	5A	C_L = 15 pF, R_L = 400 Ω		24	40	ns
$t_{pd0(D-\overline{Q})}$	Propagation delay time from D input to $\overline{Q}$ output	5A	C_L = 15 pF, R_L = 400 Ω		7	15	ns
$t_{pd1(C-Q)}$	Propagation delay time from clock input to Q output	5A	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(C-Q)}$	Propagation delay time from clock input to Q output	5A	C_L = 15 pF, R_L = 400 Ω		7	15	ns
$t_{pd1(C-\overline{Q})}$	Propagation delay time from clock input to $\overline{Q}$ output	5A	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(C-\overline{Q})}$	Propagation delay time from clock input to $\overline{Q}$ output	5A	C_L = 15 pF, R_L = 400 Ω		7	15	ns

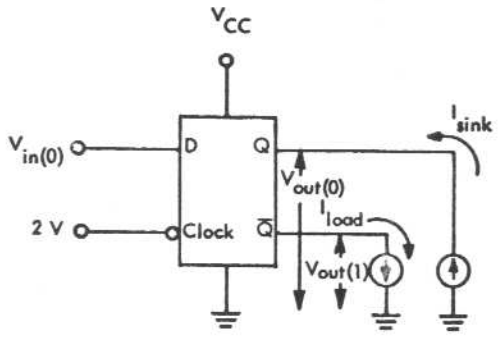
† These typical times indicate that period occurring prior to the 1.5 V level of clock pulse t_0 during which data at the D input will still be recognized.

d-c test circuits†



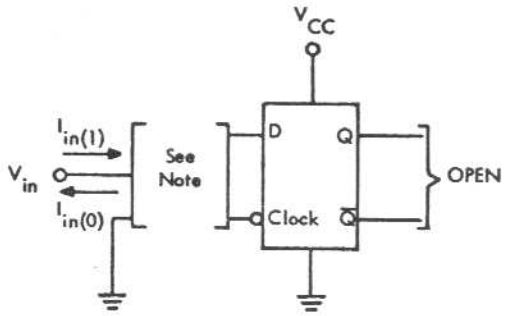
1. Each output is tested separately.

FIGURE 1



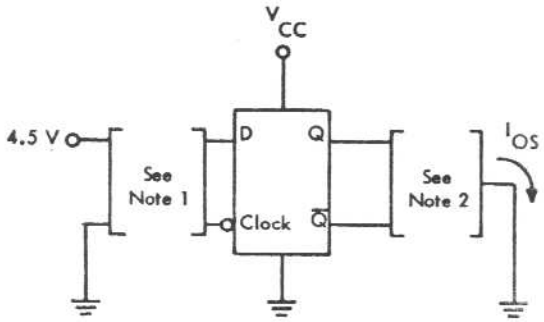
1. Each output is tested separately.

FIGURE 2



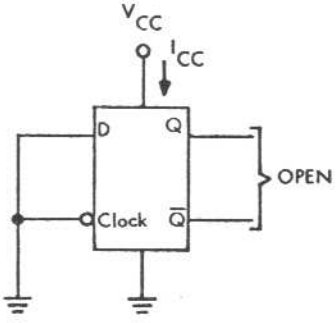
1. Each input is tested separately.
2. When testing $I_{in(1)}$ at D ground clock.
3. When testing $I_{in(1)}$ at clock ground all D inputs.

FIGURE 3



1. Input conditions are in accordance with truth table depending on output under test.
2. Each latch and each input is tested separately.

FIGURE 4



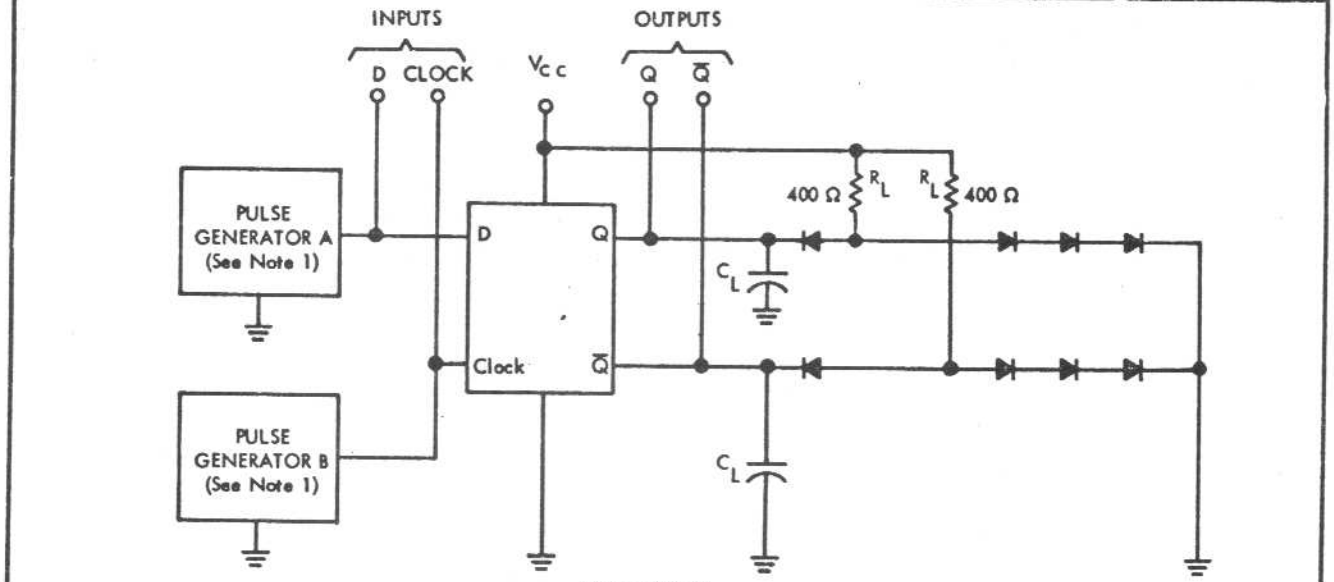
1. All latches are tested simultaneously.

FIGURE 5

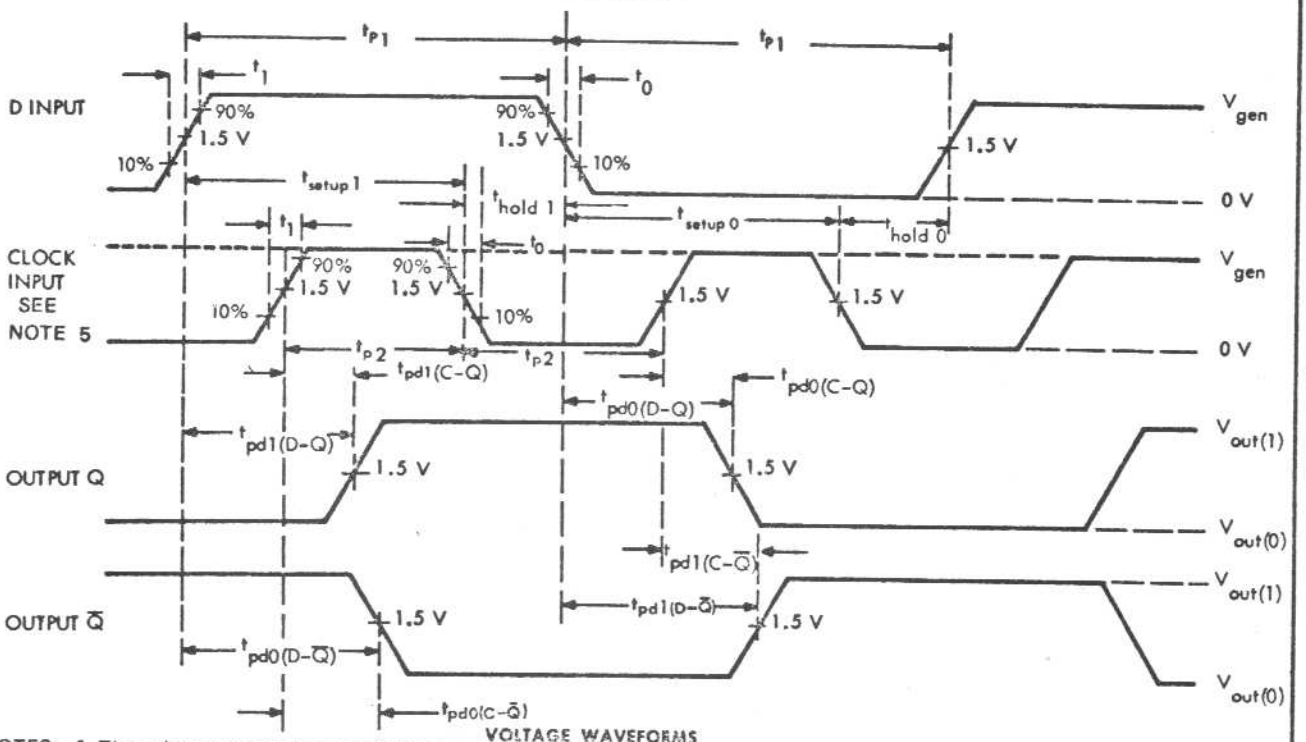
† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, and $Z_{out} \approx 50\Omega$. For pulse generator A t_{p1} = 1 μs and PRR = 500 kHz. For pulse generator B, t_{p2} = 500 ns and PRR = 1 MHz. Positions of D-input and clock-input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916.
5. When measuring t_{pd1} (D-Q), t_{pd0} (D-Q), t_{pd0} (D-$\overline{Q}$) and t_{pd1} (D-$\overline{Q}$) clock input must be held at logical 1.

FIGURE 5A — SN7475N SWITCHING TIMES

temporary storage of binary data

This application demonstrates the use of the SN7475N bistable latch as a temporary storage of binary-coded decimal data, from the SN7490N decade counter, which is to be decoded by the SN7441N decoder/driver. Temporary storage is desirable at this point for two reasons:

a. At counting frequencies above several cycles per second, it is sometimes desirable to eliminate the flicker on the display tube caused by reading an input count which is too fast to be recognized.

b. During the time that the latch is storing information the decade counter may start acquiring data for the next display.

A typical sequence of operation is illustrated (see figure 6):

1. During t_1, reset decade counter to 0. At end of t_1, indicator will display "0".
2. During t_2, count BCD 3 at output of SN7490N. Indicator still displays "0".
3. At start of t_3, indicator will display "3". At end of t_3, BCD 3 is committed to memory by SN7475N and the SN7490N may begin counting again.
4. During t_4, reset decade counter to 0 and count BCD 5 at output of SN7490N. Indicator still displays "3".
5. At start of t_5, indicator will display "5". At end of t_5, BCD 5 is committed to memory by SN7475N and the SN7490N is released . . . .

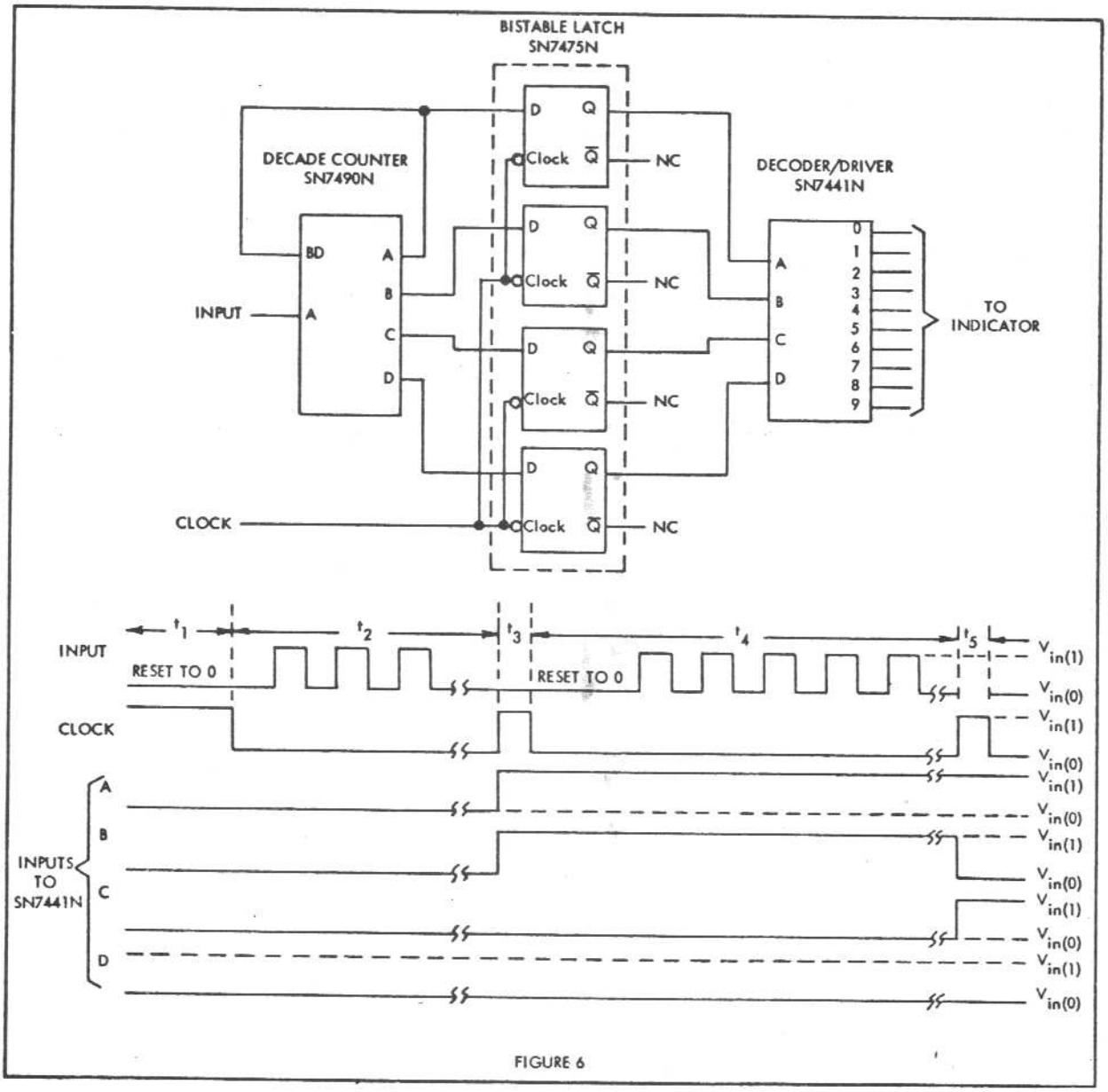


FIGURE 6

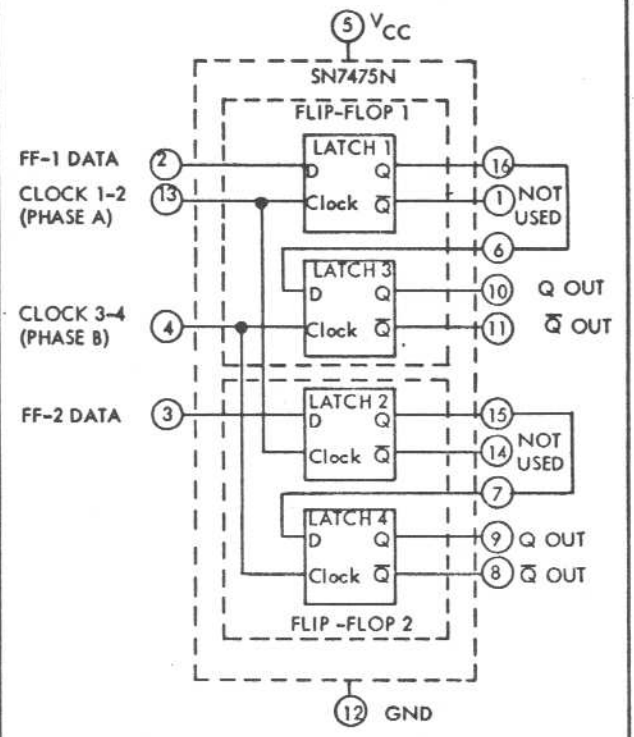
TYPICAL APPLICATION

dual D-type master-slave flip-flop

This application demonstrates the use of the SN7475N as a dual D-type master-slave flip-flop, provided that two-phase clocking is permissible. Each of the D-type flip-flops are formed by merely interconnecting the Q output of one of the latches (which serves as the master) to the data input of another latch (which serves as the slave). Each of these interconnected latches must have a separate clock line; therefore if a dual D-type master-slave flip-flop is constructed from a single package (see figure 7) they must be operated synchronously.

A typical transfer of data is illustrated. Note that after the start of t_1 the data input is released to acquire new information as the master section has "locked up" the original data after clock pulse A_1. At the start of t_2 the data "locked up" in the master is transferred to the output, and at the end of t_2 (and for the duration of t_3) the slave retains the original data.

This type of flip-flop is desirable in applications where speed is not a primary requirement and where the additional clock skew, resulting from this delay between the two clock pulses, affords greater system reliability.



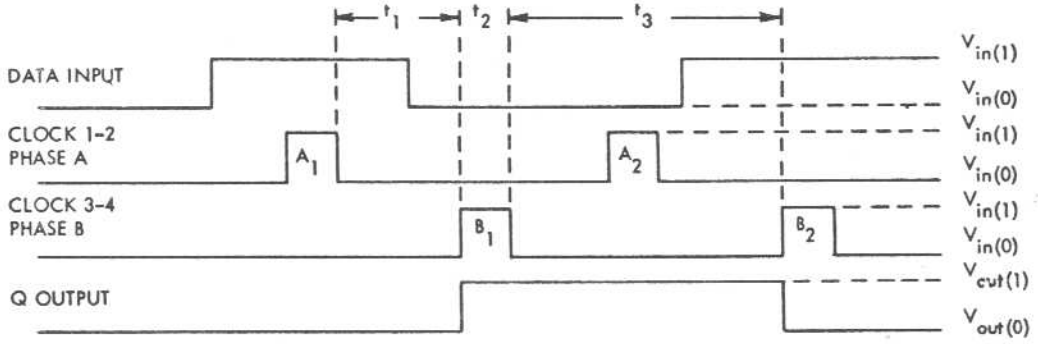


FIGURE 7

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Dual Master/Slave Flip-Flop with Pre-Set and Clear

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 4

4. MANUFACTURER'S NAME AND PART NO.

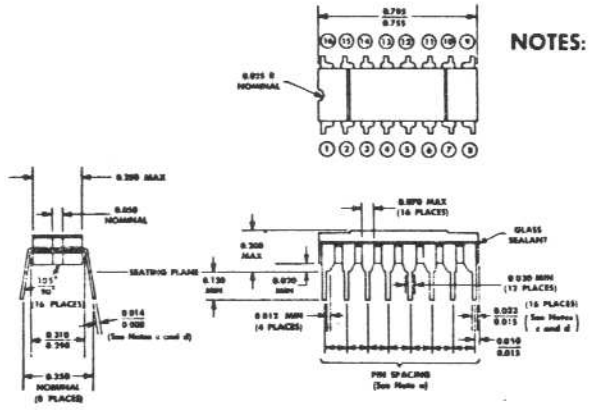
Texas Instrument, Part No. SN7476N
Sprague Part No. USN7476B
National Semiconductor Corp. Part No. DM8500N
Motorola Part No. MC7476P

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED REMOVE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES PLATING APPLY AFTER PLATING TOLERANCES ON FRACTIONS: ± 1/64 DECIMALS : ± .005 ANGLES : ± 1/2° MATERIAL: # FINISH: #	WORK AUTH NO.	FOXBORO THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.	
	DRAFTSMAN B Walker — DATE 3/24/69	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7476N	
	DESIGNER		
	CHECKER B Walker — 3/24/69		
	ENGINEER — 5/1/69	SIZE A — SYMBOL — DRAWING NO. V3008FB — REV A	
	RELEASED		
	LOCAL RELEASE	SCALE: NONE — SHEET 1 OF 4	

FORM 8033A (6/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (1) and (16)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

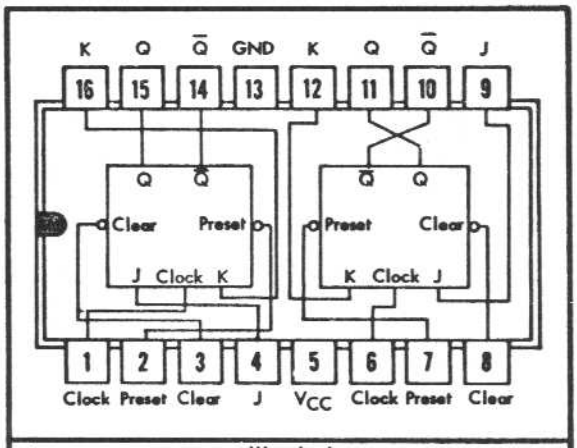
d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

16-PIN FUNCTIONS

logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES:
1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.



positive logic
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Clear and preset are independent from clock

description

The SN7476N J-K flip-flop is based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows (see figure 1):

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

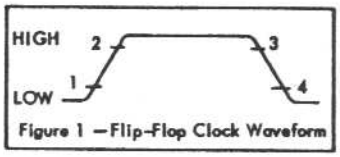
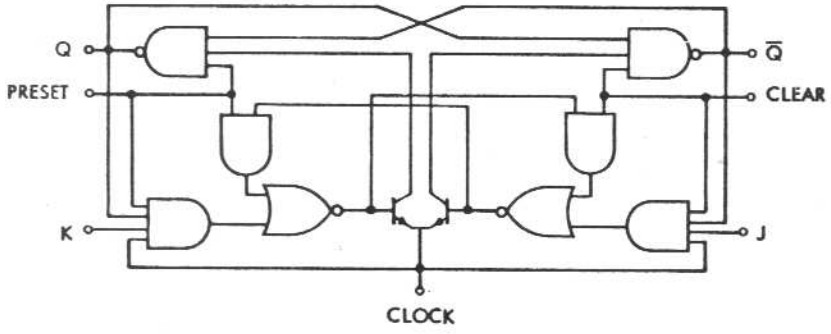


Figure 1 —Flip-Flop Clock Waveform

functional block diagram (each flip-flop)



recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output, N . . . . . 1 to 10
Width of Clock Pulse, $t_{p(clock)}$ . . . . . ≥ 20 ns
Width of Clear or Preset Pulse . . . . . ≥ 25 ns
Input Setup Time, t_{setup} . . . . . ≥ Applied Clock Pulse Width
Input Hold Time, t_{hold} . . . . . ≥ 0

electrical characteristics, T_A = 0°C to 70°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{In(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = 4.75 V	2			V
$V_{In(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = 4.75 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = 4.75 V, I_{load} = −400 μA	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = 4.75 V, I_{sink} = 16 mA		0.22‡	0.4	V
$I_{In(0)}$	Logical 0 level input current at J or K	V_{CC} = 5.25 V, V_{In} = 0.4 V			−1.6	mA
$I_{In(0)}$	Logical 0 level input current at clear, preset, or clock	V_{CC} = 5.25 V, V_{In} = 0.4 V			−3.2	mA
$I_{In(1)}$	Logical 1 level input current at J or K	V_{CC} = 5.25 V, V_{In} = 2.4 V			40	μA
		V_{CC} = 5.25 V, V_{In} = 5.5 V			1	mA
$I_{In(1)}$	Logical 1 level input current at clear, preset, or clock	V_{CC} = 5.25 V, V_{In} = 2.4 V			80	μA
		V_{CC} = 5.25 V, V_{In} = 5.5 V			1	mA
I_{OS}	Short-circuit output current†	V_{CC} = 5.25 V, V_{In} = 0	−18		−57	mA
I_{CC}	Supply current (each flip flop)	V_{CC} = 5 V, V_{In} = 5 V		8		mA

†Not more than one output should be shorted at a time.
‡These Typical values are at V_{CC} = 5 V, and T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, and N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	C_l = 15 pF	10	15		MHz
t_{pd1}	Propagation delay time to logical 0 level from clear or preset to output	C_l = 15 pF		26	50	ns
t_{pd0}	Propagation delay time to logical 1 level from clear or preset to output	C_l = 15 pF		34	50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_l = 15 pF	10	26	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_l = 15 pF	10	34	50	ns

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Full Adder

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheets 5,6,7,8,9,10 & 11

4. MANUFACTURER'S NAME AND PART NO.

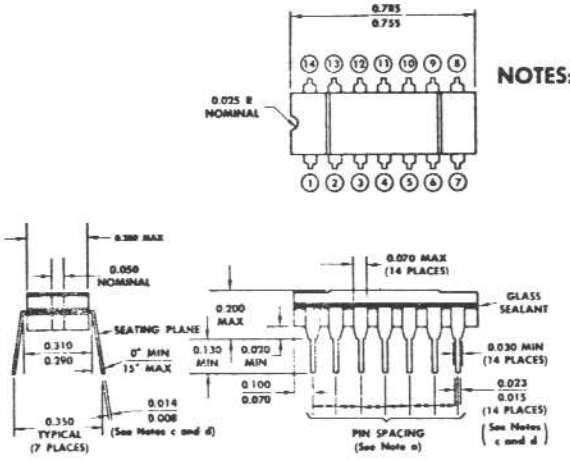
Texas Instrument, Part No. SN7480N
Sprague Part No. USN7480A

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.	FOXBORO	THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
REMOVE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES TOLERANCING APPLY AFTER PLATING	CRAFTSMAN E. Wallace 7/24/69		
	DESIGNER	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7480N	
TOLERANCES ON FRACTIONS: ± 1/64 DECIMALS: ± .005 ANGLES: ± 1/2°	CHECKER E. Wallace 7/24/69		
MATERIAL: N/A	ENGINEER J. Wood 3/20/69	SIZE A	SYMBOL
FINISH: N/A	RELEASE	DRAWING NO. V3008FC	REV A
	LOCAL RELEASE	SCALE: NONE	SHEET 1 OF 11

FORM 8088A (8/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

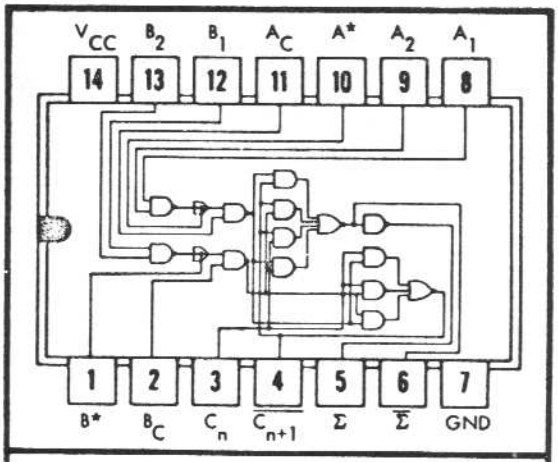
14-PIN FUNCTIONS

logic

TRUTH TABLE (See Notes 1, 2, and 3)

C_n	B	A	$\overline{C_{n+1}}$	$\overline{\Sigma}$	Σ
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

NOTES: 1. $A = \overline{A\bigstar \cdot A_C}$, $B = \overline{B\bigstar \cdot B_C}$
where $A\bigstar = \overline{A_1 \cdot A_2}$, $B\bigstar = \overline{B_1 \cdot B_2}$
2. When $A\bigstar$ or $B\bigstar$ are used as inputs, A_1 and A_2 or B_1 and B_2 respectively must be connected to GND.
3. When A_1 and A_2 or B_1 and B_2 are used as inputs, $A\bigstar$ or $B\bigstar$ respectively must be open or used to perform Dot-OR logic.



positive logic

See truth table

description

The SN7480 is a single-bit, high-speed, binary full adder with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output. Designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit (see schematic diagram) utilizes diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs. The circuit is entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V

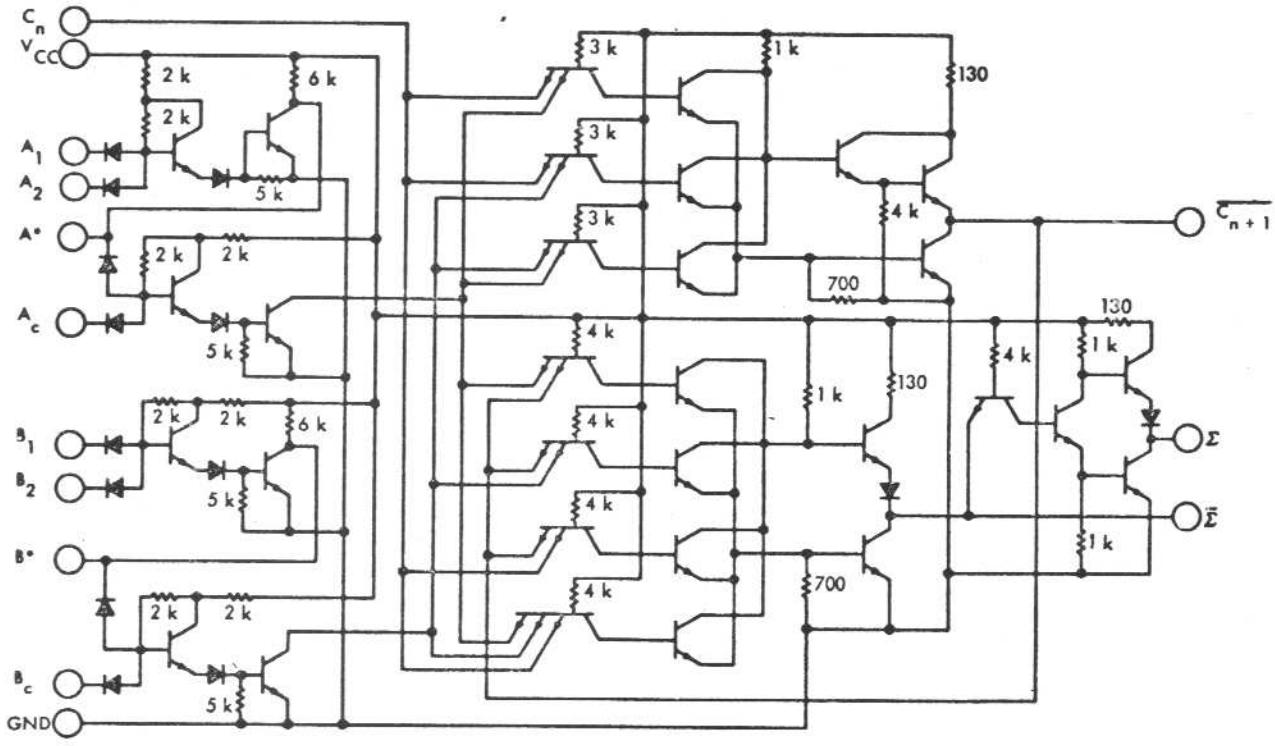
Maximum Allowable Fan-Out From Outputs:

$\overline{C_{n+1}}$, N . . . . . 1 to 5

Σ or $\overline{\Sigma}$, N . . . . . 1 to 10

A★ or B★, N . . . . . 1 to 3

schematic diagram

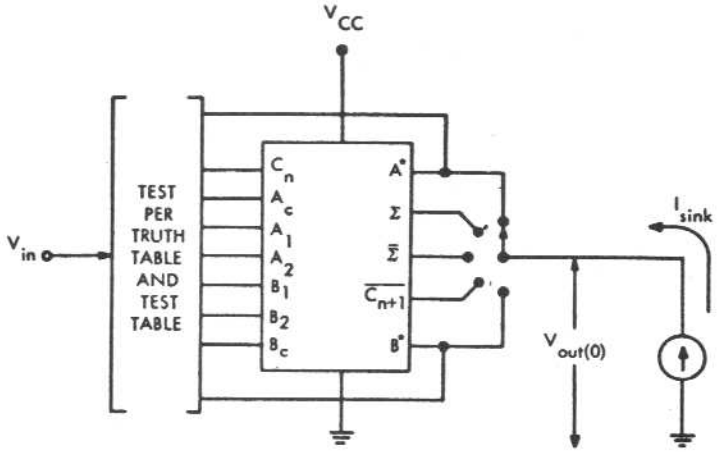


Component values shown are nominal.
Resistor values are in ohms.

THE FOXBORO COMPANY SYSTEMS DIVISION	V3008 FC	Rev. A
	Sheet of	

5039 (6/68)

d-c test circuits § (continued)

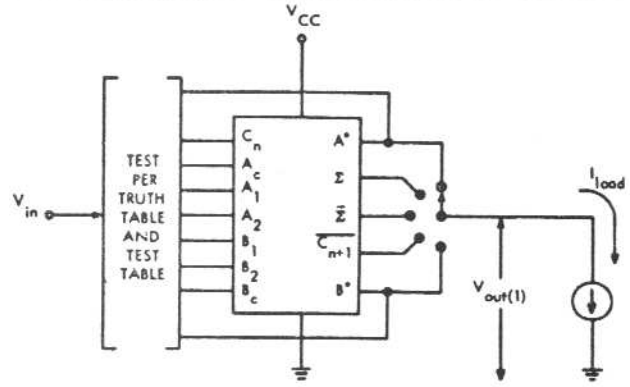


TEST TABLE

Output Under Test	I_{sink} (Min)
Σ or $\overline{\Sigma}$	16 mA
$\overline{C_{n+1}}$	8 mA
A★ or B★	4.8 mA

1. Each input or output is tested separately.
2. When A★ is tested A_1 and A_2 are at GND. When B★ is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 is tested, A★ or B★ respectively, is open.

FIGURE 42



TEST TABLE

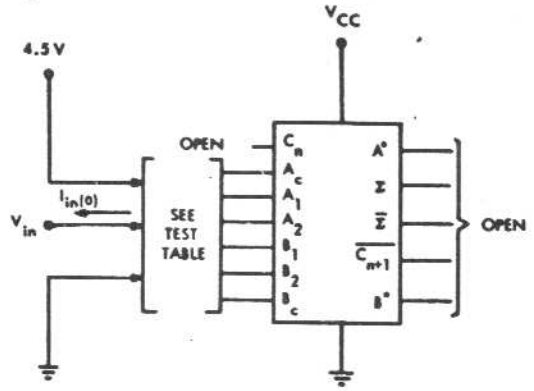
Output Under Test	I_{load} (Min)
Σ or $\overline{\Sigma}$	-400 μA
$\overline{C_{n+1}}$	-200 μA
A★ or B★	-120 μA

1. Each input or output is tested separately.
2. When A★ is tested A_1 and A_2 are at GND. When B★ is tested B_1 and B_2 are at GND.
3. When A_1 and A_2 or B_1 and B_2 are tested A★ or B★, respectively, is open.

FIGURE 43

§Arrows indicate actual direction of current flow.

d-c test circuits§(continued)

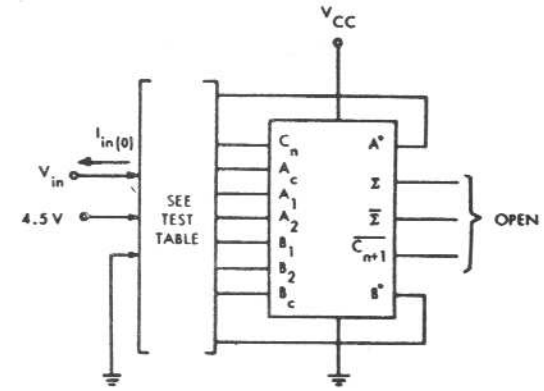


TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	GND
A_1	A_2	None
A_2	A_1	None
B_1	B_2	None
B_2	B_1	None
A_c	None	A_1 and A_2
B_c	None	B_1 and B_2

1. Each input is tested separately.

FIGURE 44



TEST TABLE

Apply V_{in} (Test $I_{in(0)}$)	Apply 4.5 V	GND
A★	A_c	A_1 and A_2
B★	B_c	B_1 and B_2
C_n	None	None

Unused inputs are open.

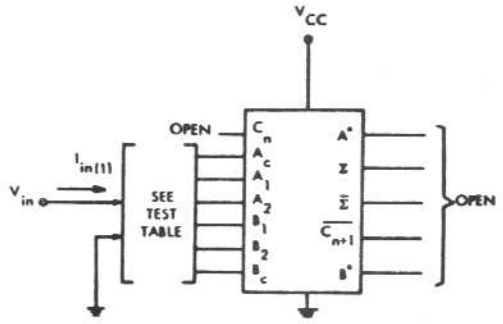
1. Each input is tested separately.

FIGURE 45

§Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§(continued)



TEST TABLE

Apply V_{in} (Test $i_{in(1)}$)	GND
A_1	A_2
A_2	A_1
B_1	B_2
B_2	B_1
A_c	A★
B_c	B★

1. Each input is tested separately.

FIGURE 46

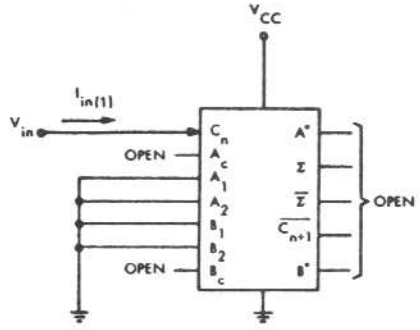
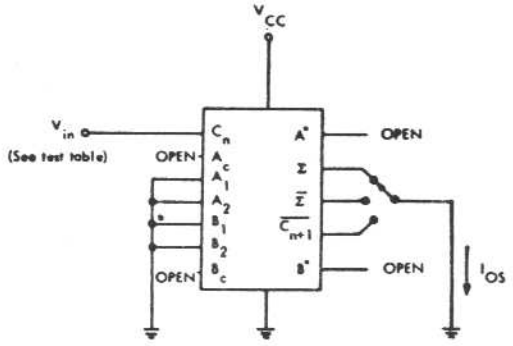


FIGURE 47



1. Each output is tested separately.

TEST TABLE

Output Under Test	V_{in} Value
Σ	V_{CC}
$\overline{\Sigma}$ or $\overline{C_{n+1}}$	GND

FIGURE 48

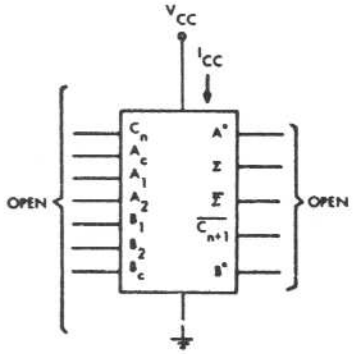


FIGURE 49

§ Arrows indicate actual direction of current flow.

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	42 and 43	$V_{CC} = 4.75$ V, $V_{in(0)} = 0.8$ V, $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V	2			V
$V_{in(0)}$	Logical 0 input voltage	42 and 43	$V_{CC} = 4.75$ V, $V_{in(1)} = 2$ V, $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	43	$V_{CC} = 4.75$ V	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	42	$V_{CC} = 4.75$ V		0.22‡	0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_2, B_1, B_2, A_c or B_c	44	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at A★ or B★	45	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−2.6	mA
$I_{in(0)}$	Logical 0 level input current at C_n	45	$V_{CC} = 5.25$ V, $V_{in} = 0.4$ V			−8	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_2, B_1, B_2, A_c or B_c	46	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			15	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
$I_{in(1)}$	Logical 1 level input current at C_n	47	$V_{CC} = 5.25$ V, $V_{in} = 2.4$ V			200	μA
			$V_{CC} = 5.25$ V, $V_{in} = 5.5$ V			1	mA
I_{OS}	Short-circuit output current at Σ or $\overline{\Sigma}$†	48	$V_{CC} = 5.25$ V	−18		−57	mA
I_{OS}	Short-circuit output current at $\overline{C_{n+1}}$†	48	$V_{CC} = 5.25$ V	−18		−70	mA
I_{CC}	Supply current	49	$V_{CC} = 5$ V		21‡		mA

†Not more than one output should be shorted at a time.
‡These typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

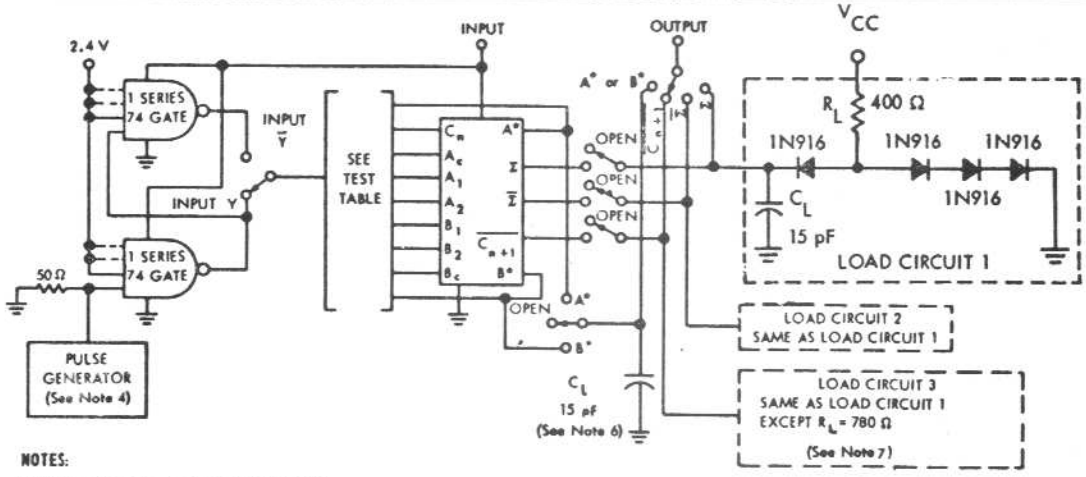
switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER ¶	FROM INPUT	TO OUTPUT	FIGURE 57 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_n	$\overline{C_{n+1}}$	1	N = 5		13	17	ns
t_{pd0}			2	N = 5		8	12	ns
t_{pd1}	B_C	$\overline{C_{n+1}}$	3	N = 5		18	25	ns
t_{pd0}			4	N = 5		38	55	ns
t_{pd1}	A_C	Σ	5	N = 10		52	70	ns
t_{pd0}			6	N = 10		62	80	ns
t_{pd1}	B_C	$\overline{\Sigma}$	7	N = 10		38	55	ns
t_{pd0}			8	N = 10		56	75	ns
t_{pd1}	A_1	A★	9	$C_L = 15$ pF		48	65	ns
t_{pd0}			10	$C_L = 15$ pF		17	25	ns
t_{pd1}	B_1	B★	11	$C_L = 15$ pF		48	65	ns
t_{pd0}			12	$C_L = 15$ pF		17	25	ns

¶t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

PARAMETER MEASUREMENT INFORMATION

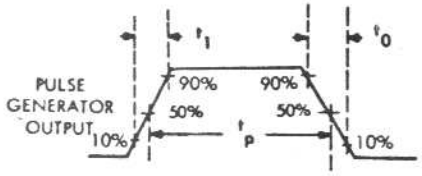
switching characteristics (continued)



NOTES:

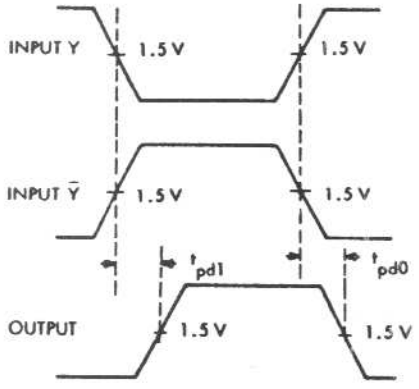
1. Perform test in accordance with test table.
2. Each output is tested separately.
3. Voltage values are with respect to network GND terminal.
4. The generator has the following characteristics: $V_{gen} = 3$ V, $t_1 = t_0 \leq 15$ ns, $t_p = 0.5\ \mu s$, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
5. Inputs and outputs not otherwise specified are open.
6. C_L and C_1 include probe and jig capacitance.
7. Load circuit 3 simulates output load of 5.

TEST CIRCUIT



TEST TABLE (See Note 5)

TEST NO.	OUTPUT UNDER TEST	APPLY INPUT $\overline{Y}$ TO	APPLY INPUT Y TO	APPLY + 2.4 V TO	APPLY GND TO	APPLY OUTPUT LOADING TO
1	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
2	$\overline{C_{n+1}}$	None	C_n	None	B_1	$\overline{C_{n+1}}$ (N = 5)
3	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
4	$\overline{C_{n+1}}$	B_c	None	C_n	A_1, B_1	$\overline{C_{n+1}}$ (N = 5)
5	Σ	A_c	None	C_n	A_1, B_1	Σ (N = 10) $\overline{\Sigma}$ (N = 10) $\overline{C_{n+1}}$ (N = 5)
6	Σ	A_c	None	C_n	A_1, B_1	Σ (N = 10) $\overline{\Sigma}$ (N = 10) $\overline{C_{n+1}}$ (N = 5)
7	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
8	$\overline{\Sigma}$	B_c	None	C_n	B_1	$\overline{\Sigma}$ (N = 10)
9	A★	None	A_1	A_2	None	A★ (C_L = 15 pF)
10	A★	None	A_1	A_2	None	A★ (C_L = 15 pF)
11	B★	None	B_1	B_2	None	B★ (C_L = 15 pF)
12	B★	None	B_1	B_2	None	B★ (C_L = 15 pF)



VOLTAGE WAVEFORMS

FIGURE 57 -- SN7480 SWITCHING TIMES

TYPICAL APPLICATIONS

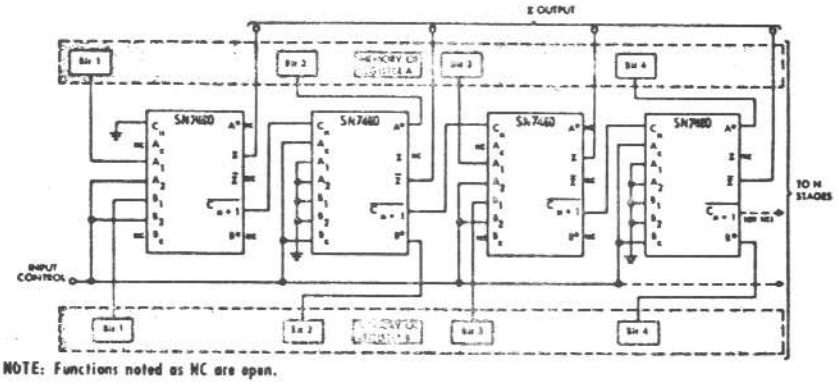
n-bit binary adder or subtractor (see figures F and G)

The SN7480 is designed specifically for N-bit adder or subtractor operations without external gates or inverters. In both applications, the sum or difference functions are generated in parallel while the carry functions are obtained serially. When the number of stages is small, the add or subtract time determines the maximum system clock rate. However, as the number of bits increases, the time required for the carry function to ripple through each bit becomes the limiting factor. Normally the ripple time of adders built with standard integrated circuits is excessive, and the resulting system speed is so slow that other more complex methods are required to perform these functions.

In the SN7480, two methods are used to reduce the carry delay. The carry circuit employs a high-speed Darlington output, and the logic gating has only one inversion between the C_n input and the $\overline{C_{n+1}}$ output. This logic configuration results in an inverted carry output, and consequently an inverted carry input to the succeeding stage. To counteract this inverted input without sacrificing propagation time through the carry, gates are provided within the circuit to invert the A and B inputs and the resulting sum or difference output. This interconnection method is illustrated by bit 2 and bit 4 of the adder (figure F). The inverted carry output is a *true* carry from bit 2 and bit 4, enabling the use of noninverted A and B inputs for the odd-numbered bits.

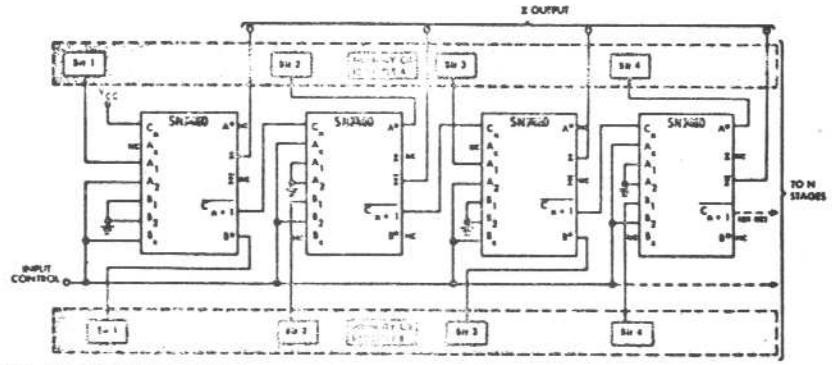
When performing subtraction (figure G) the C_n input to bit 1 is connected to a logical 1 and input bits and input control functions for the subtrahend (memory or register B) are effectively inverted.

The input control is used to disable the A and B inputs when memory or register information is being shifted. A logical 0 applied to this line will bring each sum or difference output to a logical 0 condition and maintain this level regardless of the state of the input information into each bit. For the adder (figure F), input control is applied to A_2 and B_2 of odd-numbered bits and to A_c and B_c of even-numbered bits. For the subtractor (figure G), input control is applied to A_2 and B_c of the odd-numbered bits and to A_c and B_2 of the even-numbered bits. These alternating patterns are necessary to complement the varying input sequence which they control.



NOTE: Functions noted as NC are open.

FIGURE F — N-BIT BINARY ADDER



NOTE: Functions noted as NC are open.

FIGURE G — N-BIT BINARY SUBTRACTOR

APPLICATIONS

n-bit binary adder with register selection (see Figure H)

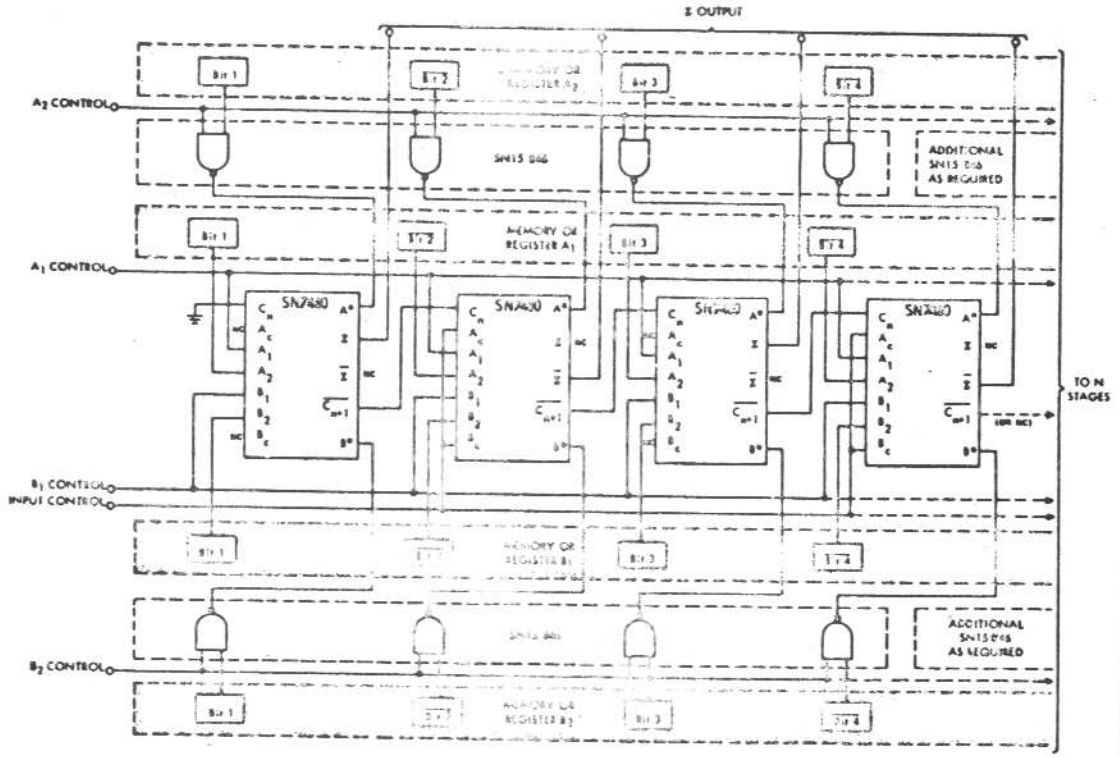
This application fully utilizes the flexibility of the input gating available within the SN7480. Two "A" registers and two "B" registers drive a single adder for each bit required. Register selection is performed internally for registers A_1 and B_1 and externally by a type SN15 846 DTL gate for registers A_2 and B_2. Dot-OR logic is performed at the A★ and B★ nodes within the adder when the register selection is made.

Operation is as follows: To add the contents of Register A_1 to Register B_1, A_2 and B_2 control lines are brought to the logical 0 state. (If the input to these lines is from a logic gate, fan-out rules should be observed.) In similar fashion, the contents of register A_1 are added to register B_2 by holding A_2 and B_1 control lines at a logical 0. Four register combinations may be used. Even-numbered input bits from each register must be inverted since the A★ and B★ inputs are being used to perform Dot-OR logic. This is not a configuration restriction for flip-flop type registers and memories, but may require additional logic elements if other storage configurations are used as inputs.

The input control function is available as in the previous application and is implemented by bringing all four register control lines and the input control line to a logical 0 level. This condition ensures a logical 0 at each Σ output regardless of "A" and "B" register logic levels.

Up to four "A" registers and four "B" registers may be implemented in a fashion analogous to that shown in figure H. Inputs from the register-control gates (SN15 846) of the additional registers would be Dot-OR connected with A_2 and B_2 registers at the A★ and B★ inputs.

To perform N-bit subtraction, the C_n input at bit 1 is connected to a logical 1 and bit inputs from each register or memory used as a subtrahend must consist of the complement of bit inputs shown for the adder addend. Input control remains the same.



NOTE: Functions noted as NC are open.

FIGURE H. N-BIT BINARY ADDER WITH REGISTER SELECTION

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
2-Bit Binary Adder

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheets 4,5,6,7,8 & 9

4. MANUFACTURER'S NAME AND PART NO.

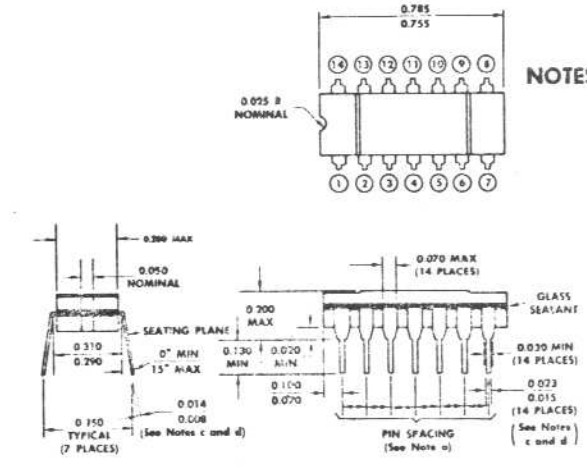
Texas Instrument, Part No. SN7482N
Sprague Part No. USN7482A

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.	FOXBORO	THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
REMOVE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES FINISH DIMS APPLY AFTER PLATING	DRAFTSMAN P. Waldron 8/24/	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN74 82N	
TOLERANCES ON FRACTIONS: ± 1/64 DECIMALS: ± .003 ANGLES: ± 1/2°	DESIGNER		
	CHECKER P. Waldron 8/24/		
MATERIAL: N/A	ENGINEER J. Kovacs 8/24/67	SIZE A	SYMBOL
FINISH: N/A	RELEASED	DRAWING NO. V3008FE	REV A
	LOCAL RELEASE	SCALE: NONE	SHEET 1 OF 9

FORM 5083A (8/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

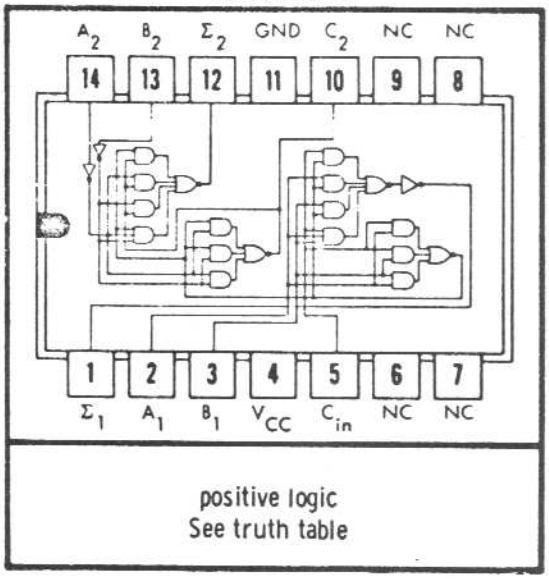
c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

TYPE SN7482N



positive logic
See truth table

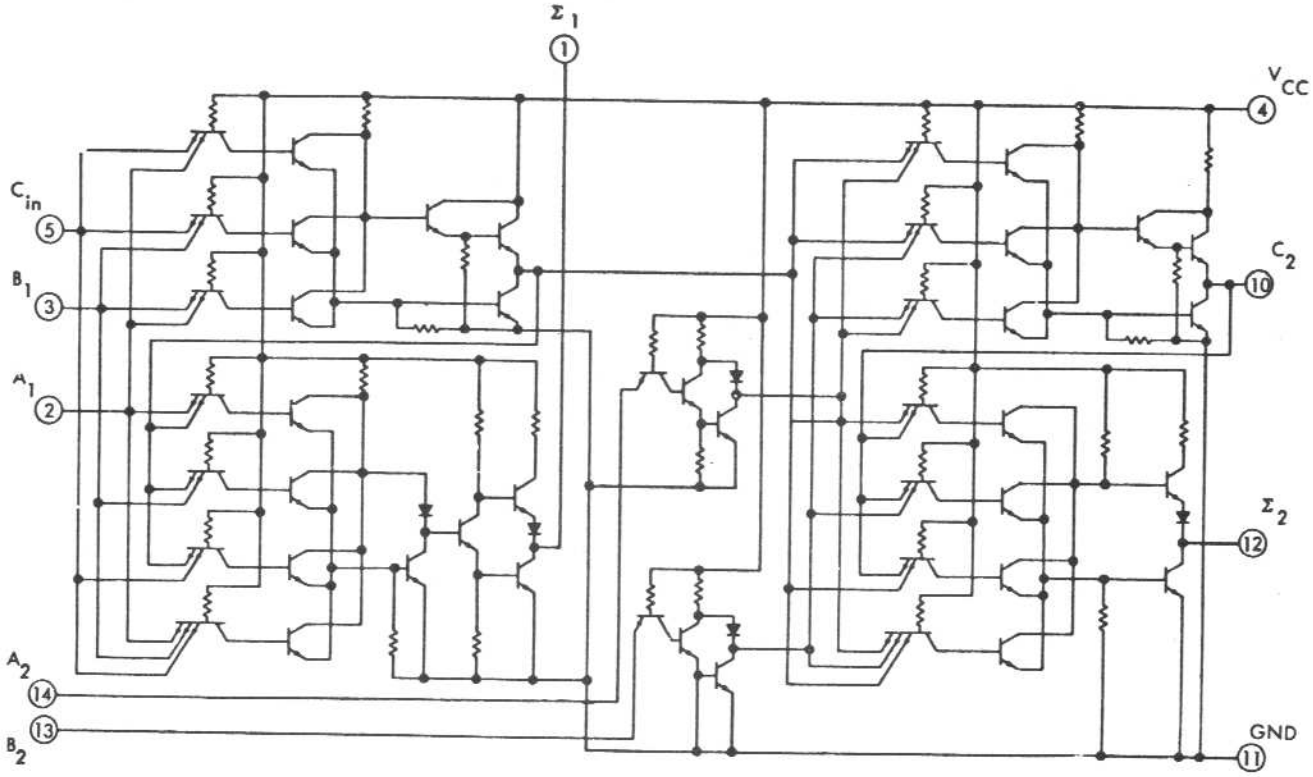
logic

TRUTH TABLE

INPUT				OUTPUT					
				WHEN C_{in} = 0			WHEN C_{in} = 1		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

description

This full adder performs the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.



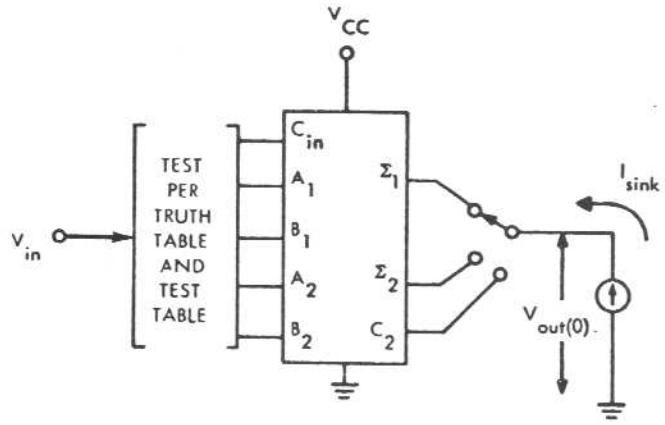
switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

PARAMETER *	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_{in}	Σ_1	1				34	ns
t_{pd0}			2				40	ns
t_{pd1}	B_2	Σ_2	3				40	ns
t_{pd0}			4				35	ns
t_{pd1}	C_{in}	Σ_2	5				38	ns
t_{pd0}			6				42	ns
t_{pd1}	C_{in}	C_2	7	N = 5		17	27	ns
t_{pd0}			8	N = 5		12	19	ns

* t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

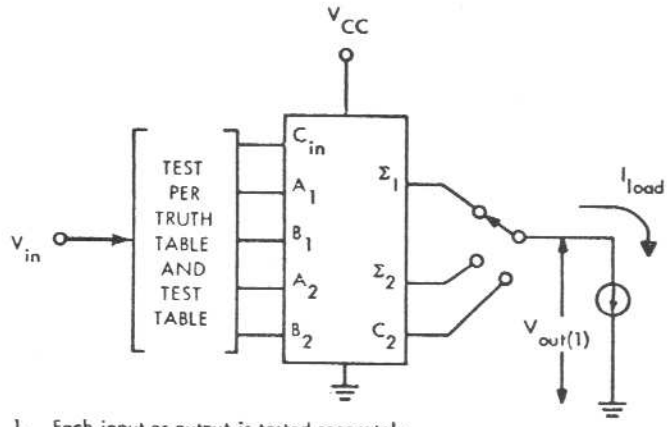


TEST TABLE

OUTPUT UNDER TEST	I_{sink}
Σ_1 or Σ_2	16 mA
C_2	8 mA

1. Each input or output is tested separately.

FIGURE 1



TEST TABLE

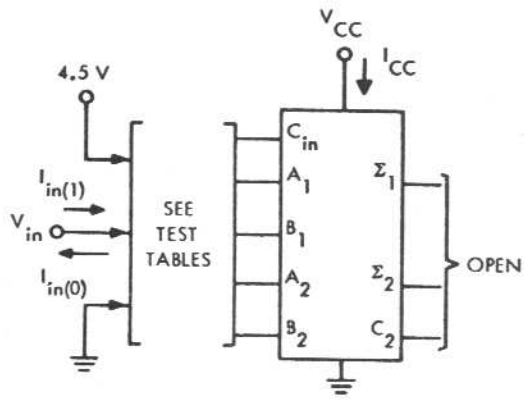
OUTPUT UNDER TEST	I_{load}
Σ_1 or Σ_2	−400 μA
C_2	−200 μA

1. Each input or output is tested separately.

FIGURE 2

†Arrows indicate actual direction of current flow.

d-c test circuits† (continued)



1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, and C_{In}; and ground B_1 and B_2.

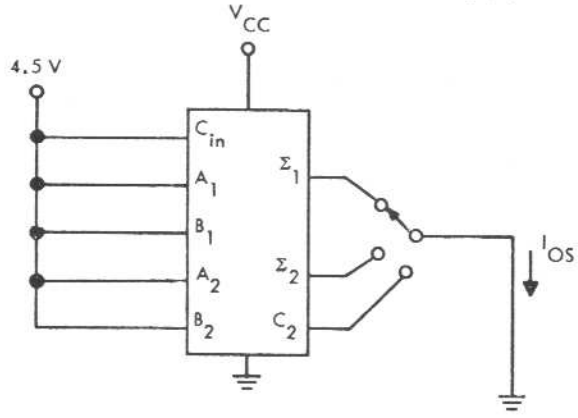
$I_{in(0)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	APPLY 4.5 V
C_{in}	A_1 and B_1
A_1	C_{in} and B_1
B_1	C_{in} and A_1
A_2	None
B_2	None

$I_{in(1)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	GND
C_{in}	A_1 and B_1
A_1	C_{in} and B_1
B_1	C_{in} and A_1
A_2	None
B_2	None

FIGURE 3



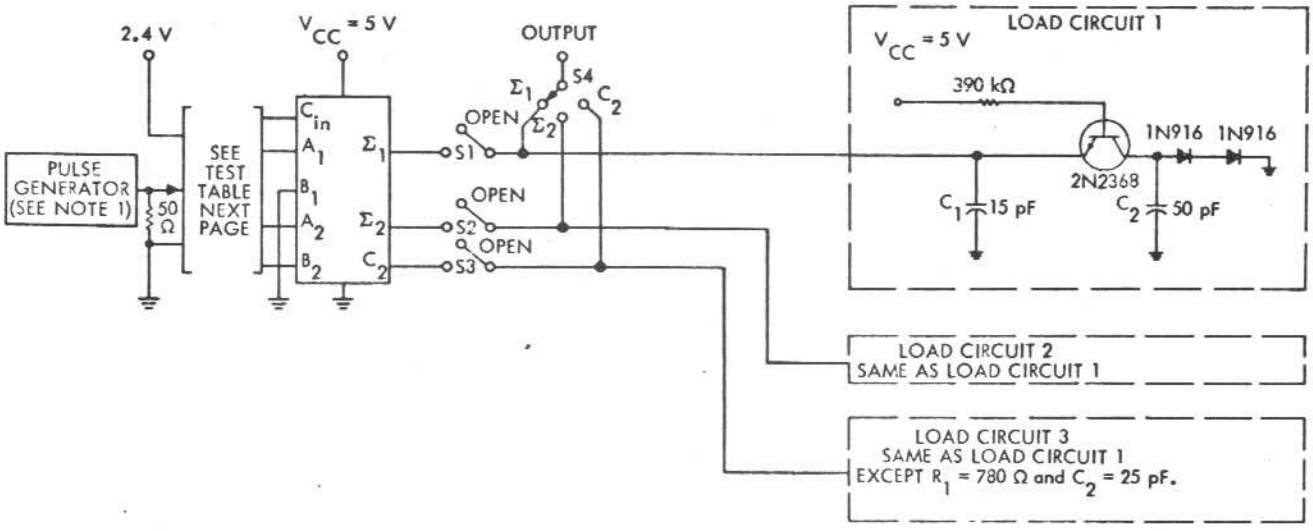
1. Each output is tested separately.

FIGURE 4

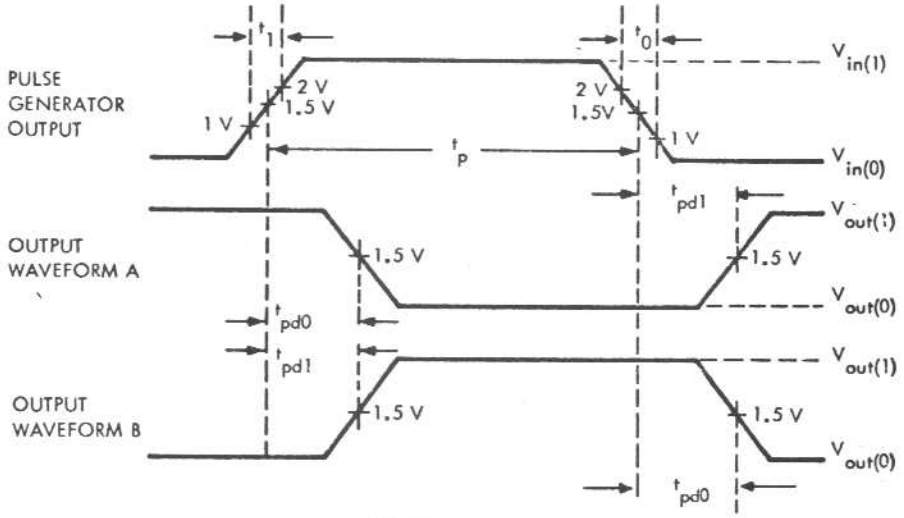
†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. The generator has the following characteristics: $V_{in(1)} \geq 2.4$V, $V_{in(0)} \leq 0.4$ V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200ns, and $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_1 includes probe and jig capacitance.

FIGURE 5. SWITCHING TIMES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V

Input Voltage V_{in} (See Notes 1 and 2) . . . . . 5.5 V

Operating Free-Air Temperature Range . . . . . 0°C to 70°C

Storage Temperature Range (SN7482) . . . . . -65°C to 150°C

Storage Temperature Range (SN7482N) . . . . . -55°C to 125°C

NOTES:

1. These voltage values are with respect to network ground terminal.
2. Input signals must be positive with respect to network ground terminal

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V

Fan-Out From Outputs:

C_2 . . . . . 1 to 5

Σ_1 or Σ_2 . . . . . 1 to 10

electrical characteristics, T_A = 0°C to 70°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2	V_{CC} = 4.75 V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2	V_{CC} = 4.75 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 V	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 V			0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, B_1, or C_{in}	3	V_{CC} = 5.25 V, V_{in} = 0.4 V			-6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2 or B_2	3	V_{CC} = 5.25 V, V_{in} = 0.4 V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, B_1, or C_{in}	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			160	µA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at A_2 or B_2	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	µA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current at Σ_1 or Σ_2‡	4	V_{CC} = 5.25 V	-18		-55	mA
I_{OS}	Short-circuit output current at C_2‡	4	V_{CC} = 5.25 V	-18		-70	mA
I_{CC}	Supply Current	3	V_{CC} = 5 V, T_A = 25°C		35		mA

‡Not more than one output should be shorted at a time.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V

Input Voltage V_{in} (See Notes 1 and 2) . . . . . 5.5 V

Operating Free-Air Temperature Range . . . . . -55°C to 125°C

Storage Temperature Range . . . . . -65°C to 150°C

NOTES:

1. These voltage values are with respect to network ground terminal.
2. Input signals must be positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.5 V to 5.5 V

Fan-Out From Outputs:

C_2 . . . . . 1 to 5

Σ_1 or Σ_2 . . . . . 1 to 10

electrical characteristics, T_A = 55°C to 125°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2	V_{CC} = 4.5 V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2	V_{CC} = 4.5 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.5 V	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.5 V			0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, B_1, or C_{in}	3	V_{CC} = 5.5 V, V_{in} = 0.4 V			-6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2 or B_2	3	V_{CC} = 5.5 V, V_{in} = 0.4 V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, B_1, or C_{in}	3	V_{CC} = 5.5 V, V_{in} = 2.4 V			160	µA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at A_2 or B_2	3	V_{CC} = 5.5 V, V_{in} = 2.4 V			40	µA
			V_{CC} = 5.5 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current at Σ_1 or Σ_2 ‡	4	V_{CC} = 5.5 V	-20		-55	mA
I_{OS}	Short-circuit output current at C_2 ‡	4	V_{CC} = 5.5 V	-20		-70	mA
I_{CC}	Supply Current	3	V_{CC} = 5 V, T_A = 25°C		35		mA

‡ Not more than one output should be shorted at a time.

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
4-Bit Binary Adder

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheets 5,6,7,8,9 &10

4. MANUFACTURER'S NAME AND PART NO.

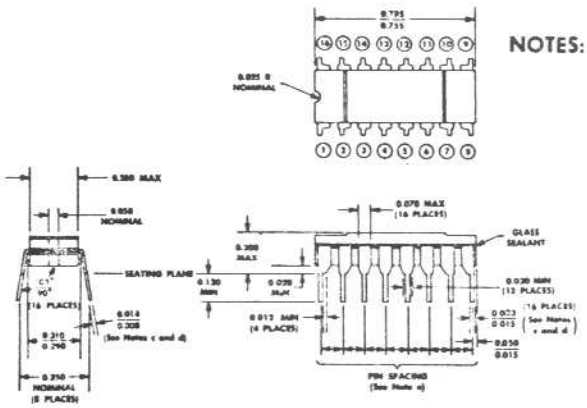
Texas Instrument, Part No. SN7483N
Sprague Part NO. USN7483B

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.		THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
REMOVE BURRS & SHARP EDGES	DRAFTSMAN	DATE	
DIMENSIONS ARE IN INCHES	DESIGNER		TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7483N
TOLERANCES APPLY AFTER PLATING	CHECKED	3/24/70	
FRACTIONS: ± 1/64 DECIMALS: ± .003 ANGLES: ± 1/2°	ENGR	3/24/70	SIZE A | SYMBOL | DRAWING NO. FV3008FF | REV A
MATERIAL: N/A	RELEASED		
FINISH: N/A	LOCAL RELEASE		SCALE: NONE | SHEET 1 OF 10

FORM 6033A (6/67)



NOTES:
a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (1) and (16)
b. All dimensions in inches unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plune.

16-PIN FUNCTIONS

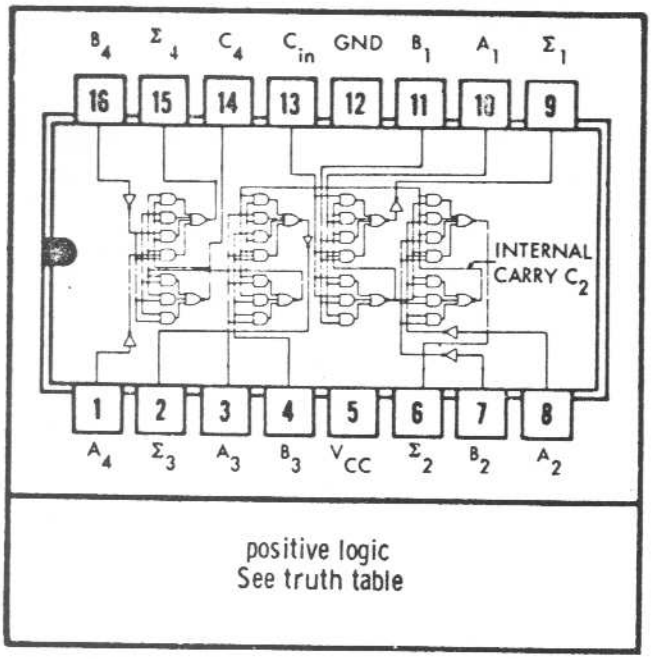
THE FOXBORO COMPANY SYSTEMS DIVISION	V3008FF
	Sheet 2 of 10

Rev. A

5033 (6/68)

TRUTH TABLE (SEE NOTE 1)

INPUT				OUTPUT					
				WHEN C_{in} = 0			WHEN C_{in} = 1		
				WHEN C_2 = 0			WHEN C_2 = 1		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

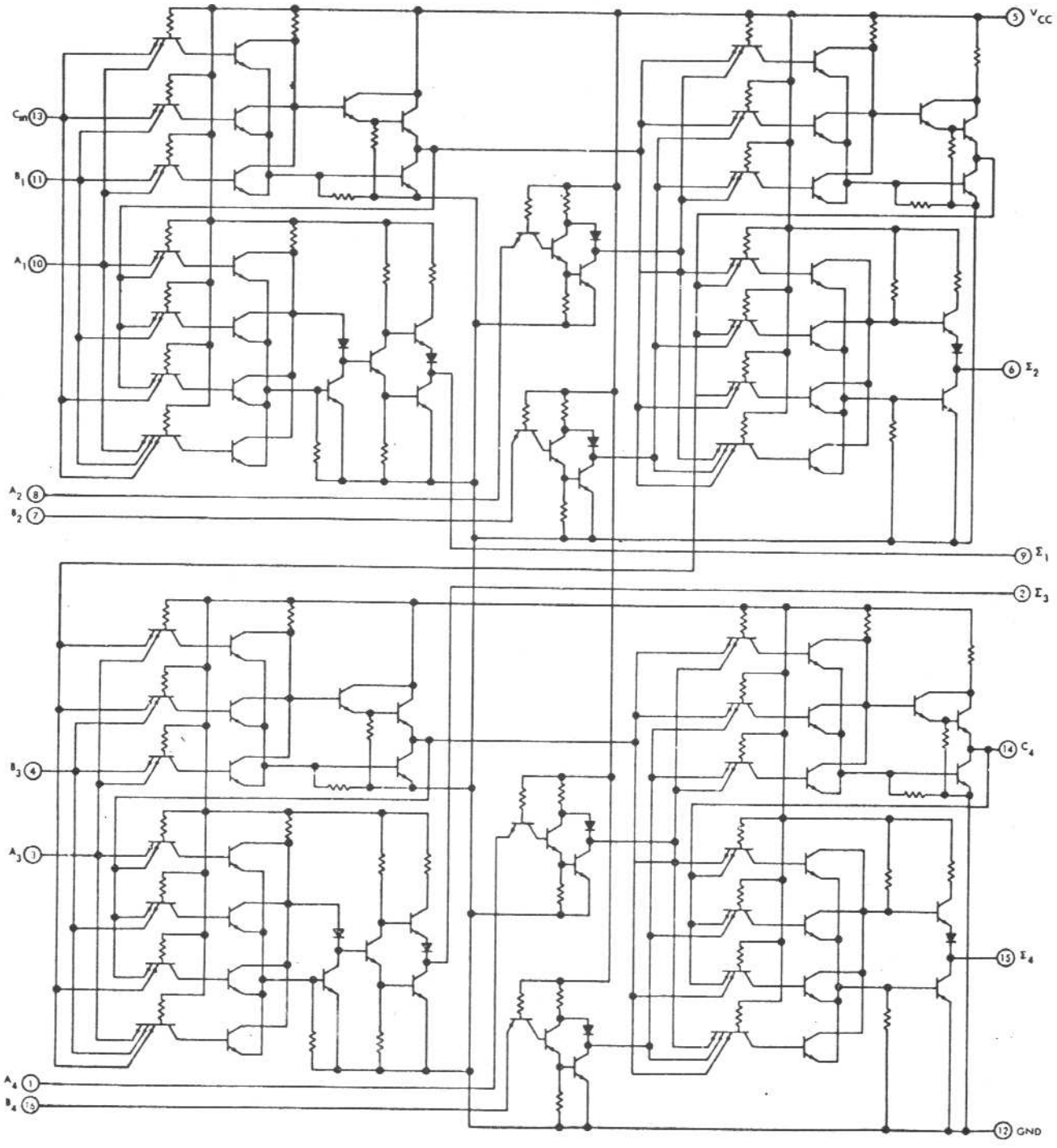


NOTE 1: Input conditions at A_1 A_2, B_1, B_2, and C_{in} are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

description

This full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform four-bit full-adder functions.

schematic



THE FOXBORO COMPANY SYSTEMS DIVISION	V3008FF	Rev. P
	Sheet 4 of 10	

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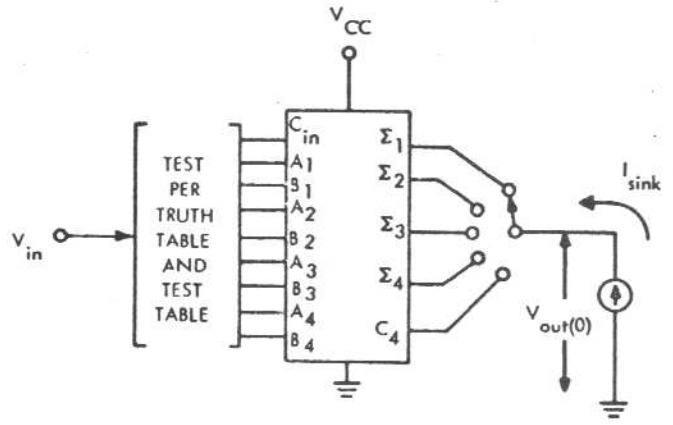
PARAMETER MEASUREMENT INFORMATION

d-c test circuits †

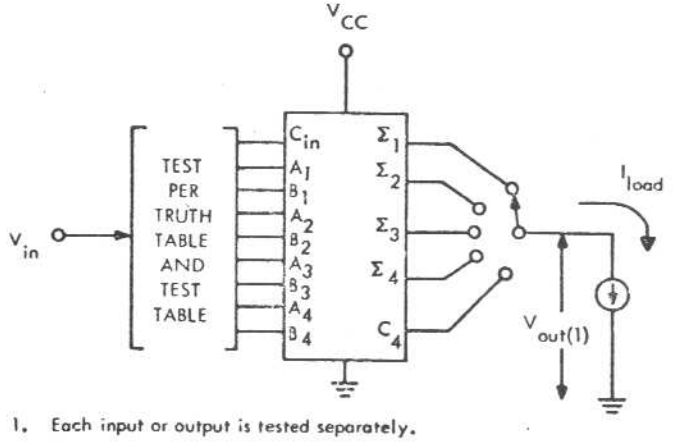


TEST TABLE

OUTPUT UNDER TEST	I_{sink}
Σ_1, Σ_2, Σ_3, or Σ_4	16 mA
C_4	8 mA

1. Each input or output is tested separately.

FIGURE 1



TEST TABLE

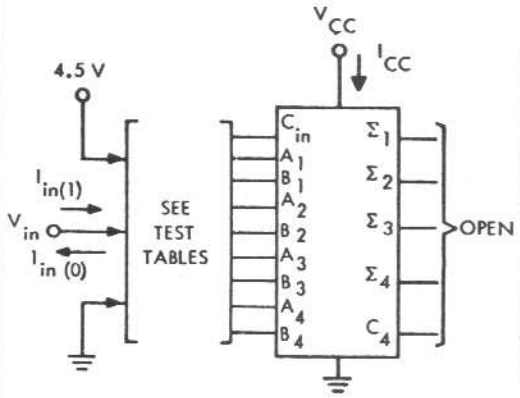
OUTPUT UNDER TEST	I_{load}
Σ_1, Σ_2, Σ_3, or Σ_4	− 400 μA
C_4	− 200 μA

1. Each input or output is tested separately.

FIGURE 2

†Arrows indicate actual direction of current flow.

d-c test circuits† (continued)



1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, A_3, A_4, and C_{in}; and ground B_1, B_2, B_3 and B_4.

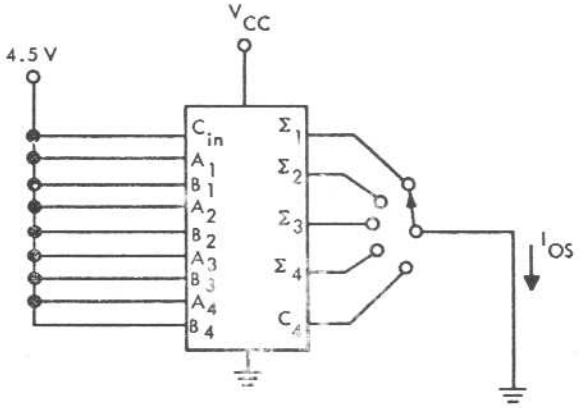
$I_{in(0)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	APPLY 4.5 V
C_{in}	A_1 and B_1
A_1	C_{in} and B_1
B_1	C_{in} and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

$I_{in(1)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	GND
C_{in}	A_1 and B_1
A_1	C_{in} and B_1
B_1	C_{in} and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

FIGURE 3

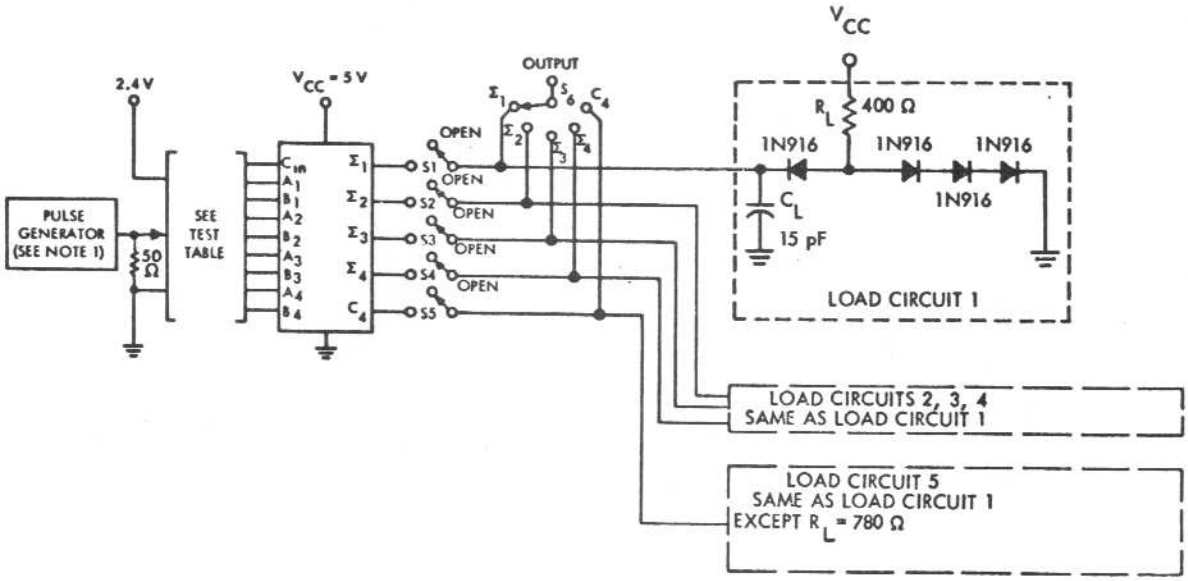


1. Each output is tested separately.

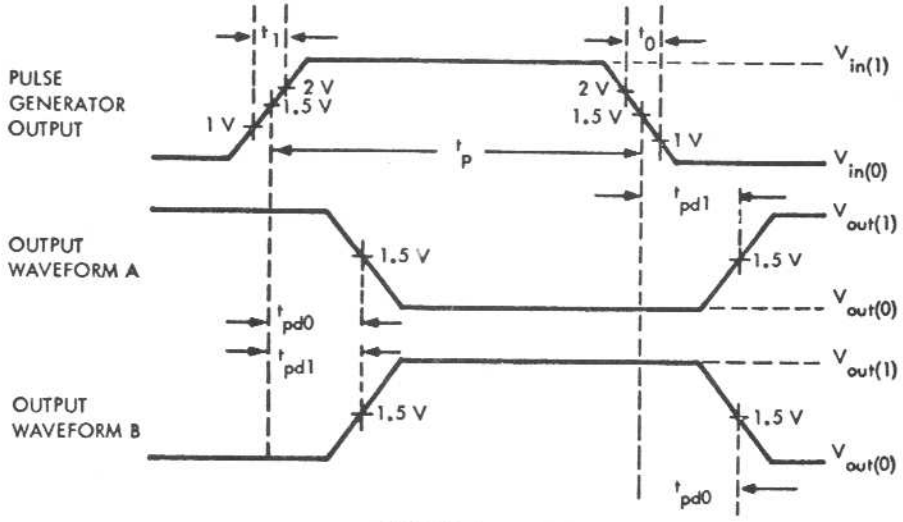
FIGURE 4

†Arrows indicate actual direction of current flow.

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES:
1. Pulse generator output pulse characteristics: $V_{in(1)} \geq$ 2.4 V, $V_{in(0)} \leq$ 0.4 V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200 ns, and $Z_{out} \approx$ 50 Ω.
2. Perform test in accordance with test table. (See sheet 2 of this figure.)
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.

FIGURE 5 – SWITCHING TIMES (SHEET 1 OF 2)

switching characteristics (continued)

TEST TABLE (SEE NOTE 6)

TEST NO.	PARA-METER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S6)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3	S4	S5
1	t_{pd1}	C_{in}	Σ_1 (WAVEFORM A)	A_1	B_1, A_2, and B_2	CLOSED	OPEN	OPEN	OPEN	OPEN
2	t_{pd0}									
3	t_{pd1}	C_{in}	Σ_2 (WAVEFORM A)	A_1 and A_2	B_1 and B_2	OPEN	CLOSED	OPEN	OPEN	OPEN
4	t_{pd0}									
5	t_{pd1}	C_{in}	Σ_3 (WAVEFORM A)	A_1, A_2, and A_3	B_1, B_2, and B_3	OPEN	OPEN	CLOSED	OPEN	OPEN
6	t_{pd0}									
7	t_{pd1}	C_{in}	Σ_4 (WAVEFORM A)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	CLOSED
8	t_{pd0}									
9	t_{pd1}	C_{in}	C_4 (WAVEFORM B)	A_1, A_2, A3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	OPEN	CLOSED
10	t_{pd0}									
11	t_{pd1}	A_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, B_2, and C_{in}	OPEN	CLOSED	OPEN	OPEN	OPEN
12	t_{pd0}									
13	t_{pd1}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2, and C_{in}	OPEN	CLOSED	OPEN	OPEN	OPEN
14	t_{pd0}									
15	t_{pd1}	A_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	OPEN
16	t_{pd0}									
17	t_{pd1}	B_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and A_4	OPEN	OPEN	OPEN	CLOSED	OPEN
18	t_{pd0}									

NOTE 6: Inputs and outputs not otherwise specified are open.

FIGURE 5 – SWITCHING TIMES (SHEET 2 OF 2)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V

Input Voltage V_{in} (See Notes 1 and 2) . . . . . 5.5 V

Operating Free-Air Temperature Range . . . . . 0°C to 70°C

Storage Temperature Range . . . . . -55°C to 125°C

NOTES:

1. These voltage values are with respect to network ground terminal.
2. Input signals must be positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V

Fan-Out From Outputs:

C_4 . . . . . 1 to 5

Σ_1, Σ_2, Σ_3, or Σ_4 . . . . . 1 to 10

electrical characteristics T_A = 0°C to 70°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2	V_{CC} = 4.75 V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2	V_{CC} = 4.75 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 V	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 V			0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_3, B_1, B_3, or C_{in}	3	V_{CC} = 5.25 V, V_{in} = 0.4 V			-6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2, A_4, B_2, or B_4	3	V_{CC} = 5.25 V, V_{in} = 0.4 V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_3, B_1, B_2, or C_{in}	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			160	µA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at A_2, A_4, B_2, or B_4	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	µA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current at Σ_1, Σ_2, Σ_3, or Σ_4 ‡	4	V_{CC} = 5.25 V	-18		-55	mA
I_{OS}	Short-circuit output current at C_4 ‡	4	V_{CC} = 5.25 V	-18		-70	mA
I_{CC}	Supply Current	3	V_{CC} = 5 V, T_A = 25°C		78		mA

‡ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N= 10)

PARAMETER §	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_{in}	1	1				34	ns
t_{pd0}			2				40	ns
t_{pd1}	C_{in}	2	3				38	ns
t_{pd0}			4				42	ns
t_{pd1}	C_{in}	3	5				50	ns
t_{pd0}			6				60	ns
t_{pd1}	C_{in}	4	7				55	ns
t_{pd0}			8				55	ns
t_{pd1}	C_{in}	C_4	9	N = 5		35	48	ns
t_{pd0}			10	N = 5		22	32	ns
t_{pd1}	A_2 or B_2	2	11 and 13				40	ns
t_{pd0}			12 and 14				35	ns
t_{pd1}	A_4 or B_4	4	15 and 17				40	ns
t_{pd0}			16 and 18				35	ns

§ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Decade Counter

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheets 4, 5, & 6

4. MANUFACTURER'S NAME AND PART NO.

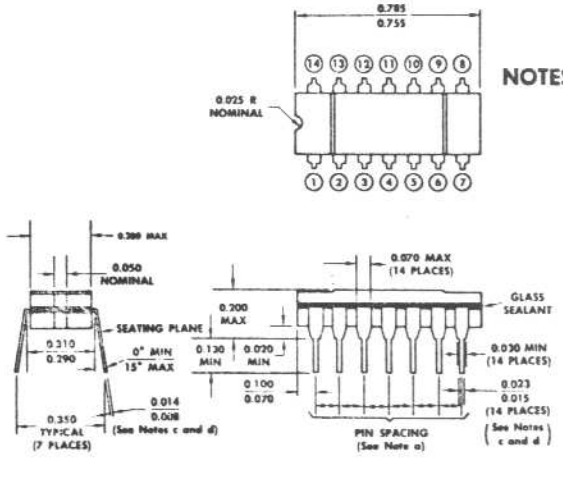
Texas Instrument, Part No. SN7490N
Sprague Part No. USN7490A
National Semiconductor Corp. Part No. DM8530N

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.	FOXBORO	THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
SHARP EDGES ARE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES TOLERANCES APPLY AFTER PLATING	DRAFTSMAN B Wallin 8/5/70	TITLE:	CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7490N
FRACTIONS ± 1/64 DECIMALS ± .005 ANGLES ± 1/2°	DESIGNER		
	CHECKED B Wallin 8/5/70		
MATERIAL: N/A	ENGINEER [illegible] 8/5/70	SIZE A	SYMBOL
FINISH: N/A	RELEASED	DRAWING NO. FV3008FK	REV A
	LOCAL RELEASE	SCALE: NONE	SHEET 1 OF 6

FORM 5063A (8/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

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	Sheet 2 of 6	

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logic

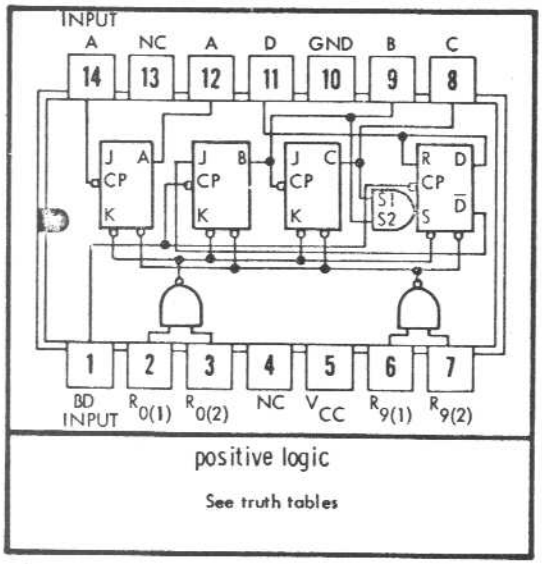
TRUTH TABLES

BCD COUNT SEQUENCE
(See Note 1)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (See Note 2)

RESET INPUTS				OUTPUT
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT



positive logic

See truth tables

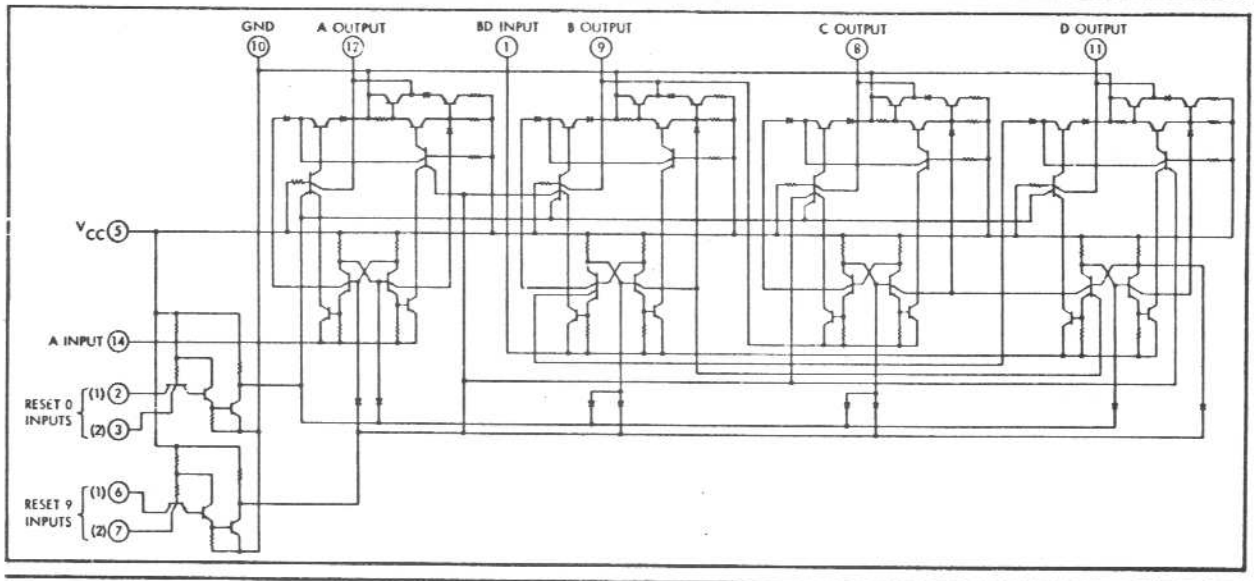
NOTES: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

description and typical count configurations

The SN7490N is a high-speed, monolithic decade counter consisting of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to a logical zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

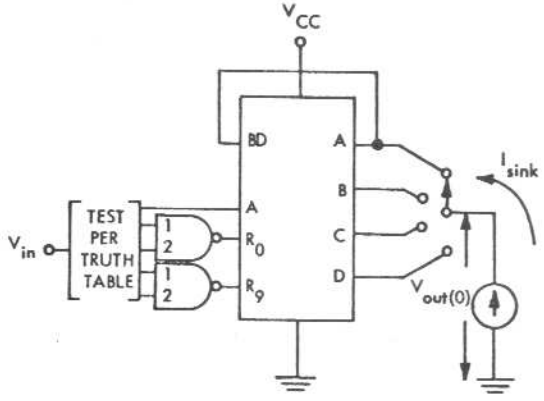
1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD 9 count for nine's compliment decimal applications.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

The SN7490N is completely compatible with Series 74 and Series 74 930 TTL, and Series 15 830 DTL logic families. Average power dissipation is 160 mW.



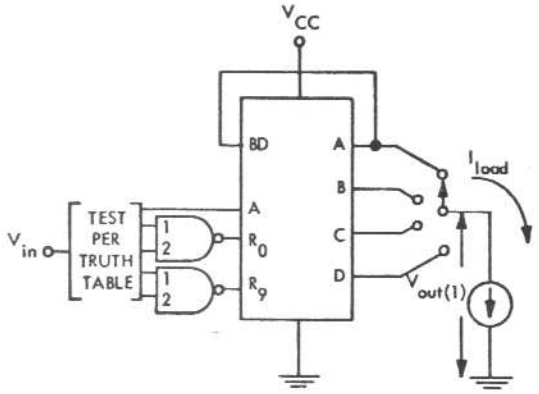
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



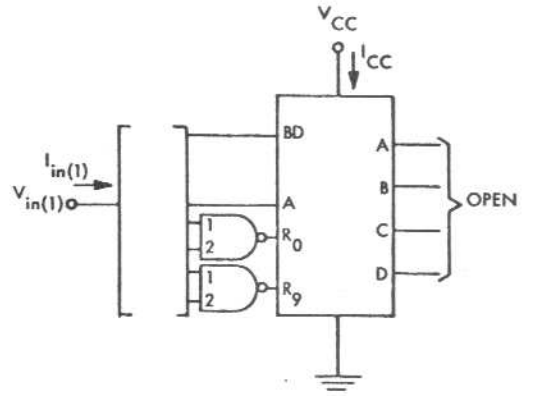
1. Each output is tested in the logical 0 state.

FIGURE 1



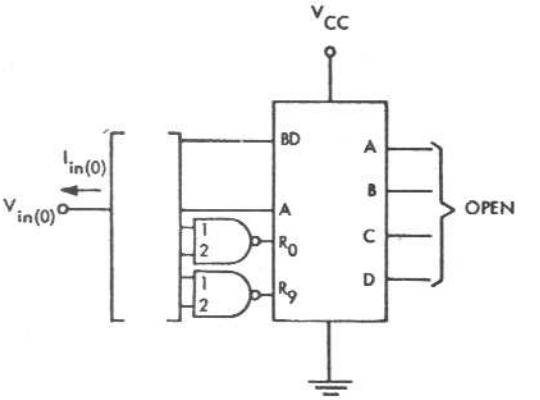
1. Each output is tested in the logical 1 state.

FIGURE 2



1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ ground $R_{0(2)}$ or $R_{9(2)}$
3. When testing $R_{0(2)}$ or $R_{9(2)}$ ground $R_{0(1)}$ or $R_{9(1)}$
4. When testing I_{CC} reset all outputs to logical 0, ground all inputs, then measure I_{CC}.

FIGURE 3



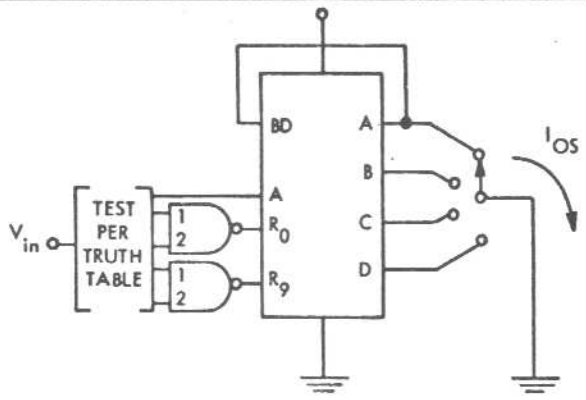
1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ apply 4.5 V to $R_{0(2)}$ or $R_{9(2)}$.
3. When testing $R_{0(2)}$ or $R_{9(2)}$ apply 4.5 V to $R_{0(1)}$ or $R_{9(1)}$.

FIGURE 4

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

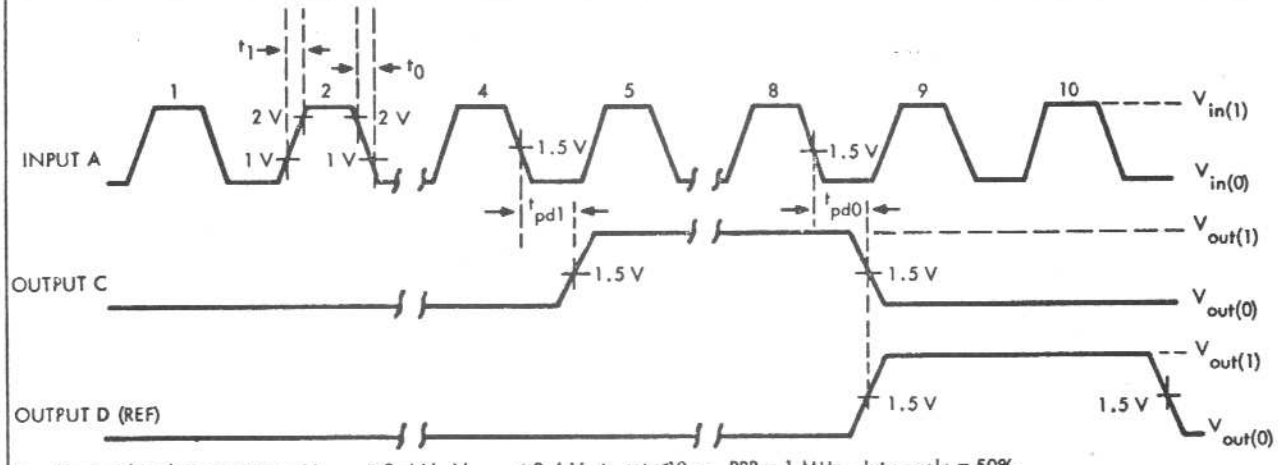


1. Each output is tested in the logical 1 state.

FIGURE 5

† Arrows indicate actual direction of current flow.

switching time voltage waveforms



1. Input pulse characterisitcs: $V_{in(1)} \geq 2.4$ V, $V_{in(0)} \leq 0.4$ V, $t_1 = t_0 \leq 10$ ns, PRR = 1 MHz, duty cycle = 50%.

FIGURE 6. SWITCHING TIME VOLTAGE WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V
Input Voltage V_{In} (See Notes 3 and 4) . . . . . 5.5 V
Operating Free-Air Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . . . -55°C to 125°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output (See Note 5) . . . . . 1 to 10
Width of Input Count Pulse, $t_{p(in)}$ . . . . . ≥ 50 ns
Width of Reset Pulse, $t_{p(reset)}$ . . . . . ≥ 50 ns

NOTE 5: Fan-out from output A to input BD and to 10 additional Series 74 loads is permitted.

electrical characteristics, T_A = 0°C to 70°C

PARAMETER		TEST FIG.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at inputs A, $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, and $R_{9(2)}$	1	V_{CC} = 4.75 V	2			V
$V_{in(1)}$	Input voltage required to ensure logical 1 at input BD	1	V_{CC} = 4.75 V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at inputs A, $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, and $R_{9(2)}$	2	V_{CC} = 4.75 V			0.8	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at input BD	2	V_{CC} = 4.75 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 V, I_{load} = -400 µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 V, I_{sink} = 16 mA			0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	µA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at input A	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			80	µA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{In(1)}$	Logical 1 level input current at input BD	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			160	µA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	4	V_{CC} = 5.25 V, V_{in} = 0.4 V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A	4	V_{CC} = 5.25 V, V_{in} = 0.4 V			-3.2	mA
$I_{In(0)}$	Logical 0 level input current at input BD	4	V_{CC} = 5.25 V, V_{in} = 0.4 V			-6.4	mA
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.25 V, V_{out} = 0 V	-18		-57	mA
I_{CC}	Supply Current	3	V_{CC} = 5 V, T_A = 25°C		32		mA

† Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIG.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses			10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output C	6			60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output C	6			60	100	ns

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
8-Bit Shift Register

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheets 5, 6 & 7

4. MANUFACTURER'S NAME AND PART NO.

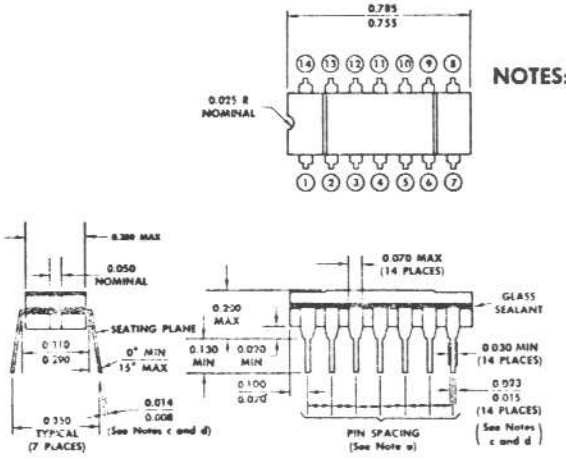
Texas Instrument, Part No. SN7491AN
Sprague Part No. USN7491A

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.	FOXBORO	THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
REMOVE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES TOLERANCES APPLY AFTER PLATING	DRAFTSMAN R. Wallace 3/9/67	TITLE:	CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7491AN
TOLERANCES ON FRACTIONS ± 1/64 DECIMALS ± .005 ANGLES ± 1/2°	DESIGNER		
	CHECKER R. Wallace 3/14/67		
MATERIAL: N/A	ENGINEER V. Dennis 3/14/67	SIZE A	SYMBOL
FINISH: N/A	RELEASED	DRAWING NO. V3009FL	REV A
	LOCAL RELEASE	SCALE: NONE	SHEET 1 OF 7

FORM 6083A (8/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11).

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

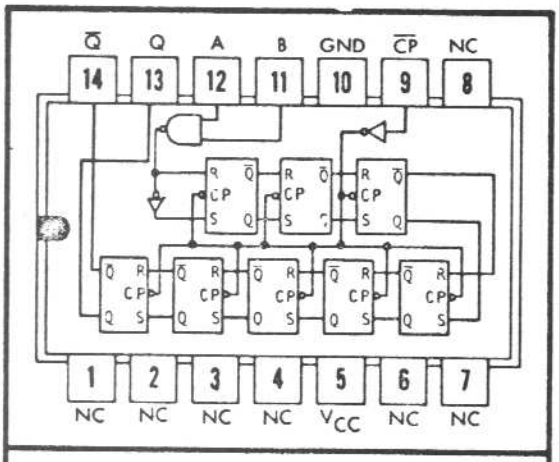
logic

TRUTH TABLE

t_n		t_{n+8}
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

NOTES: 1. t_n = bit time before clock pulse.

2. t_{n+8} = bit time after 8 clock pulses.



positive logic

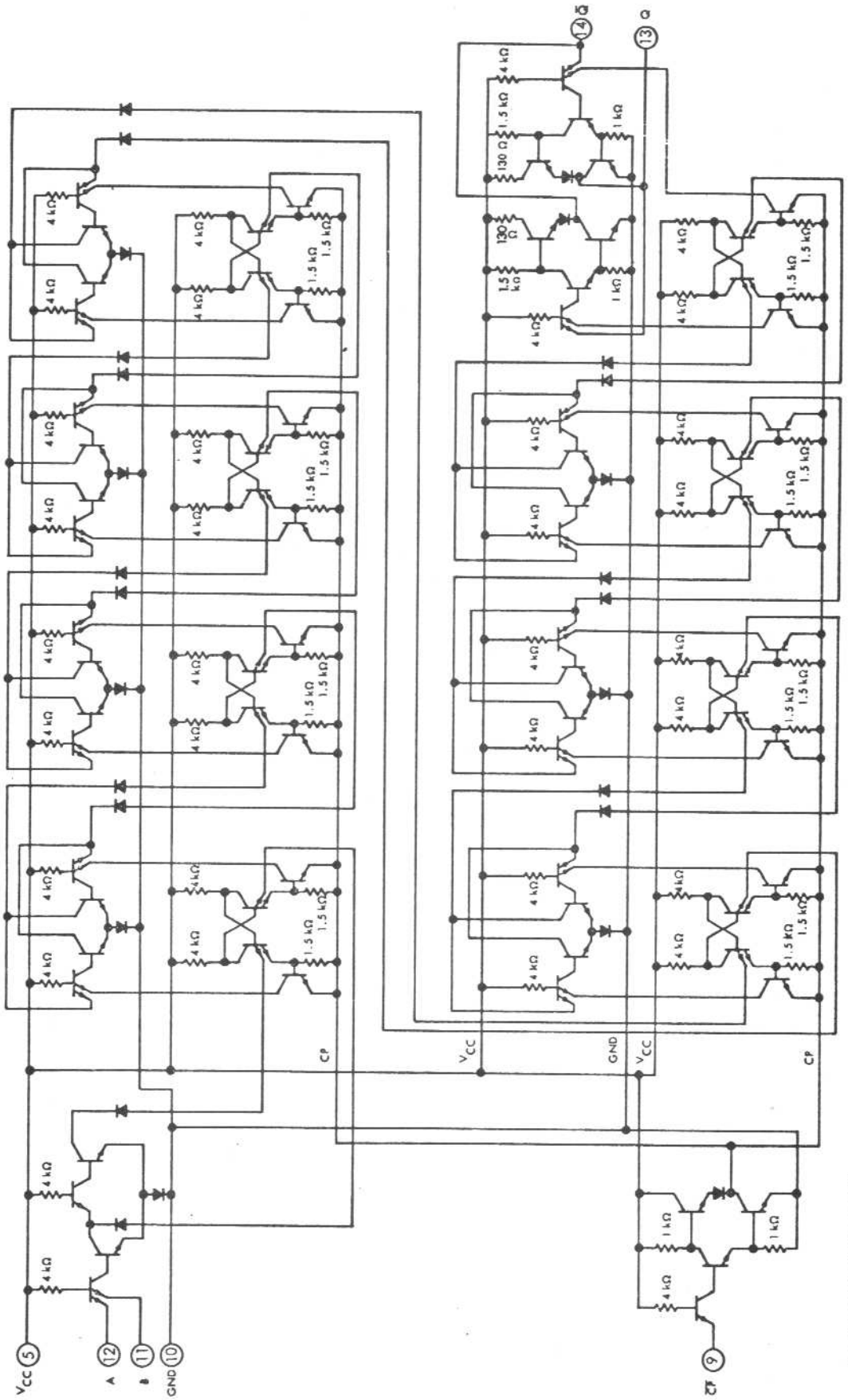
See truth table

description

The SN7491AN is a monolithic serial-in, serial-out, 8-bit shift register utilizing transistor-transistor logic (TTL) circuits in the familiar high-speed Series 54 configuration. The shift register, composed of eight R-S master-slave flip-flops, includes input gating and a clock driver. The register is capable of storing and transferring data at clock rates up to 18 MHz while maintaining a typical noise-immunity level of 1 volt. Power dissipation is typically 175 milliwatts, and full fan-out of 10 is available from the outputs.

Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. Each of the inputs (A, B and $\overline{CP}$) appear as only one TTL input load.

The clock pulse inverter/driver causes the SN7491AN to shift information to the output on the positive edge of an input clock pulse, thus enabling the shift-register to be fully compatible with the SN7470 J-K flip-flop and the SN7474 dual D-type flip-flop.



Component values shown are nominal.

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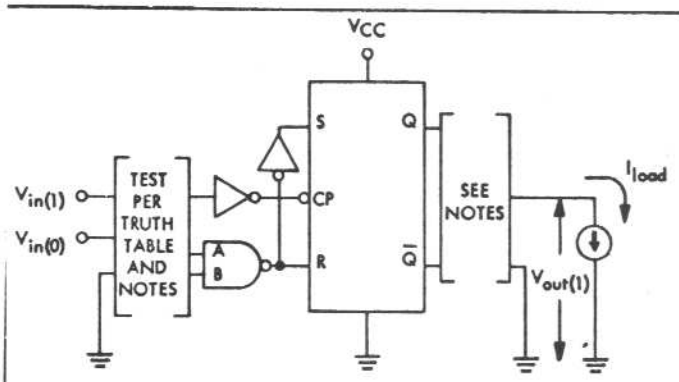
	Sheet 4 of 7	

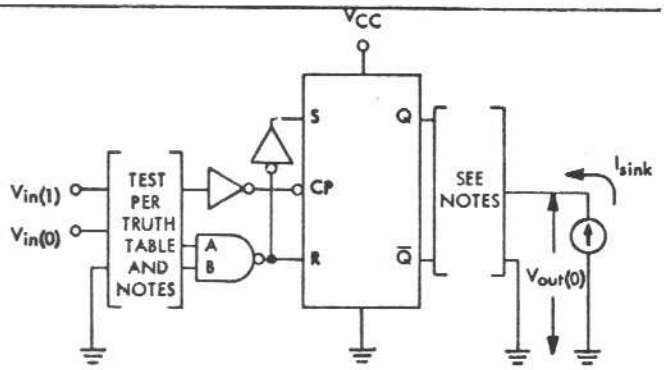
PARAMETER MEASUREMENT INFORMATION

d-c test circuits §



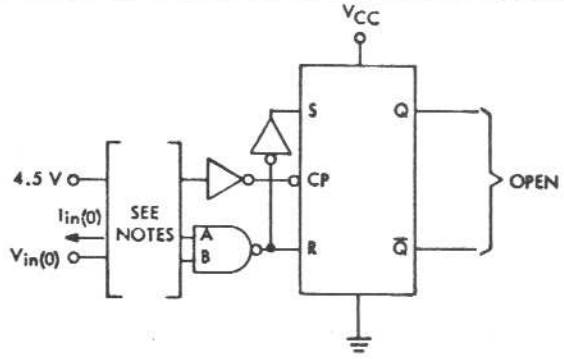
1. Each output is tested separately.
2. When testing $V_{out(1)}$ and I_{load}, ground all inputs and the unused output, then measure parameters specified.

FIGURE 1



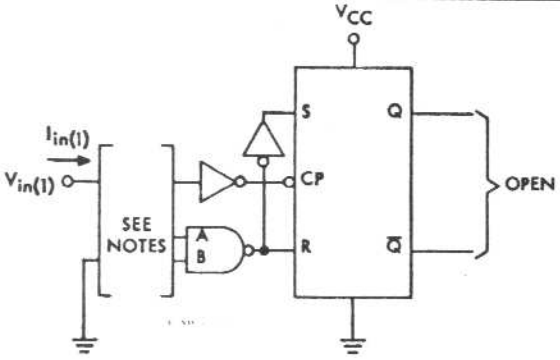
1. Each output is tested separately.
2. When testing $V_{out(0)}$ and I_{sink}, ground all inputs. Apply a momentary ground to the output to be tested then measure parameters specified.

FIGURE 2



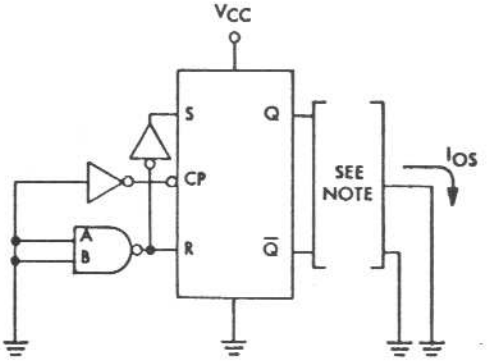
1. When testing input A apply 4.5 V to input B.
2. When testing input B apply 4.5 V to input A.

FIGURE 3



1. When testing input A ground input B.
2. When testing input B ground input A.

FIGURE 4



1. Ground the unused output then measure parameter specified.

FIGURE 5

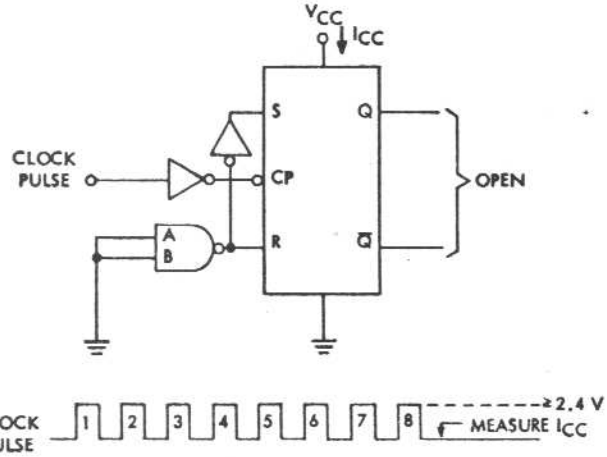
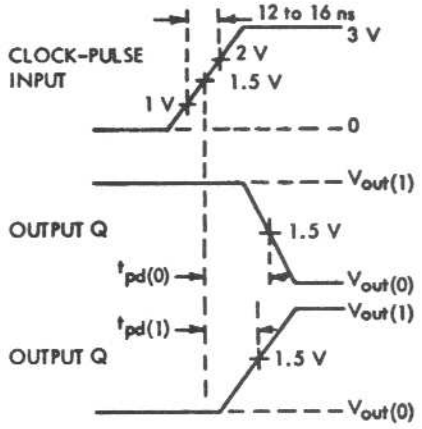


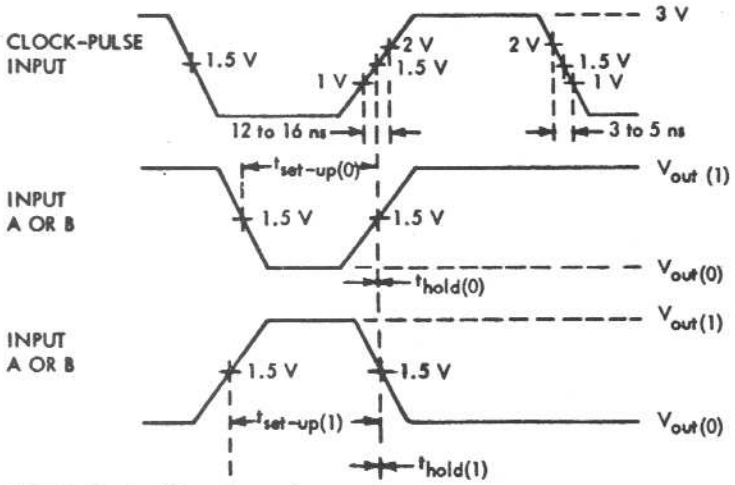
FIGURE 6

§ Arrows indicate actual direction of current flow.



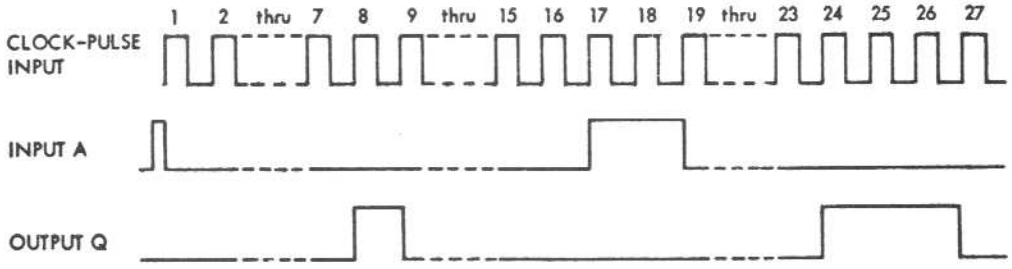
NOTE: The clock-pulse has the following characteristics: PRR = 1 MHz and duty cycle = 50%.

PROPAGATION DELAY TIMES VOLTAGE WAVEFORMS



NOTES: 1. Each input is tested separately.
2. Unused input is connected to 2.4 V
3. The clock-pulse has the following characteristics: PRR = 1 MHz and duty cycle = 50%.

SWITCHING TIMES VOLTAGE WAVEFORMS



NOTE: input B is connected to 2.4 V.

TYPICAL INPUT/OUTPUT WAVEFORMS

FIGURE 7 – SWITCHING TIMES

absolute maximum ratings over operating free-air temperature range

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V
Input Voltage V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Free-Air Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . . . -55°C to 125°C

NOTES: 3. Voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Outputs . . . . . 1 to 10

electrical characteristics, V_{CC} = 4.75 V to 5.25 V, T_A = 0 to 70°C

PARAMETER		MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage	2			V
$V_{in(0)}$	Logical 0 input voltage			0.8	V
$V_{out(1)}$	Logical 1 output voltage (N = 10)	2.4			V
$V_{out(0)}$	Logical 0 output voltage (N = 10)			0.4	V
$I_{in(1)}$	Logical 1 level input current at any input			40	μA
$I_{in(0)}$	Logical 0 level input current at any input			-1.6	mA
I_{OS}	Short-circuit output current	-18		-55	mA
I_{CC}	Supply current (T_A = 25°C)		35	70	mA

switching times, V_{CC} = 5 V, T_A = 25°C (See Figures 1 and 2)

PARAMETER		MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	10	18		MHz
$t_{p(clock)}$	Minimum clock pulse width		18	25	ns
$t_{set-up(0)}$	Minimum logical 0 level set-up time required at A or B inputs		12	25	ns
$t_{set-up(1)}$	Minimum logical 1 level set-up time required at A or B inputs		15	25	ns
$t_{hold(0)}$	Logical 0 level hold time required at A or B input†		-15	0	ns
$t_{hold(1)}$	Logical 1 level hold time required at A and B inputs		-12	0	ns
$t_{pd(1)}$	Propagation delay time to logical 1 level (clock-to-output)		24	40	ns
$t_{pd(0)}$	Propagation delay time to logical 0 level (clock-to-output)		27	40	ns

† When the unused input is at logical 1.

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
Divide by 12 Counter

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheets 4, 5, & 6

4. MANUFACTURER'S NAME AND PART NO.

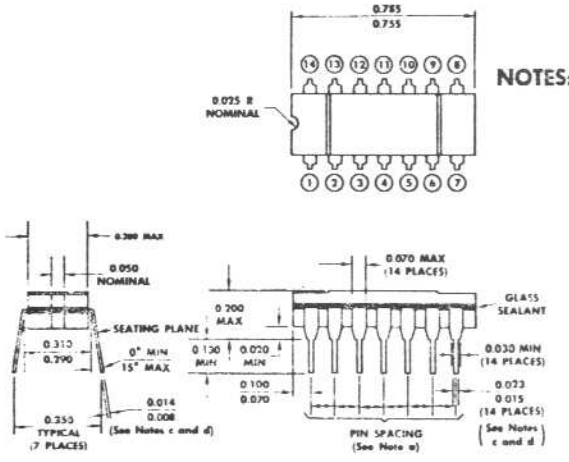
Texas Instrument, Part No. SN7492N
Sprague Part No. USN7492N
National Semiconductor Part No. DM8532N

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.	FOXBORO	THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
REMOVE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES COATINGS APPLY AFTER PLATING	DRAFTSMAN [illegible] DATE 3/24/69 DESIGNER	TITLE:	CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7492N
TOLERANCES ON FRACTIONS: ± 1/64 DECIMALS: ± .005 ANGLES: ± 1/2°	CHECKER [illegible] 3/24/69 ENGINEER [illegible] 3/24/69 RELEASED	SIZE: A	SYMBOL:	DRAWING NO.: V3008FM	REV: A
MATERIAL: #	LOCAL RELEASE	SCALE: NONE		SHEET 1 OF 6	
FINISH: #					

FORM 8093A (8/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

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		Sheet — of —

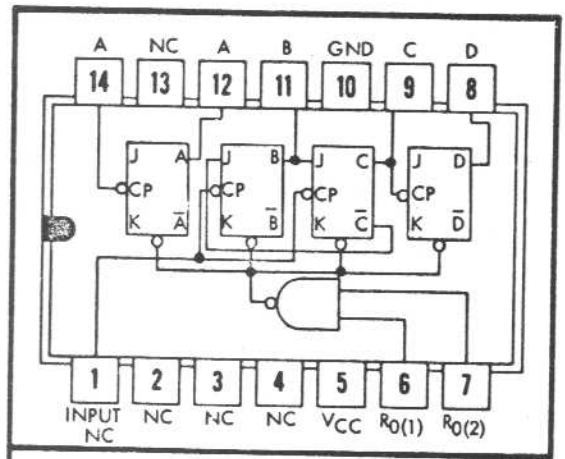
5033 (6/83)

TRUTH TABLE (See Notes 1 and 2)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	1	0	0	0
7	1	0	0	1
8	1	0	1	0
9	1	0	1	1
10	1	1	0	0
11	1	1	0	1

NOTES: 1. Output A connected to input B

2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.



Positive Logic

See Truth Table

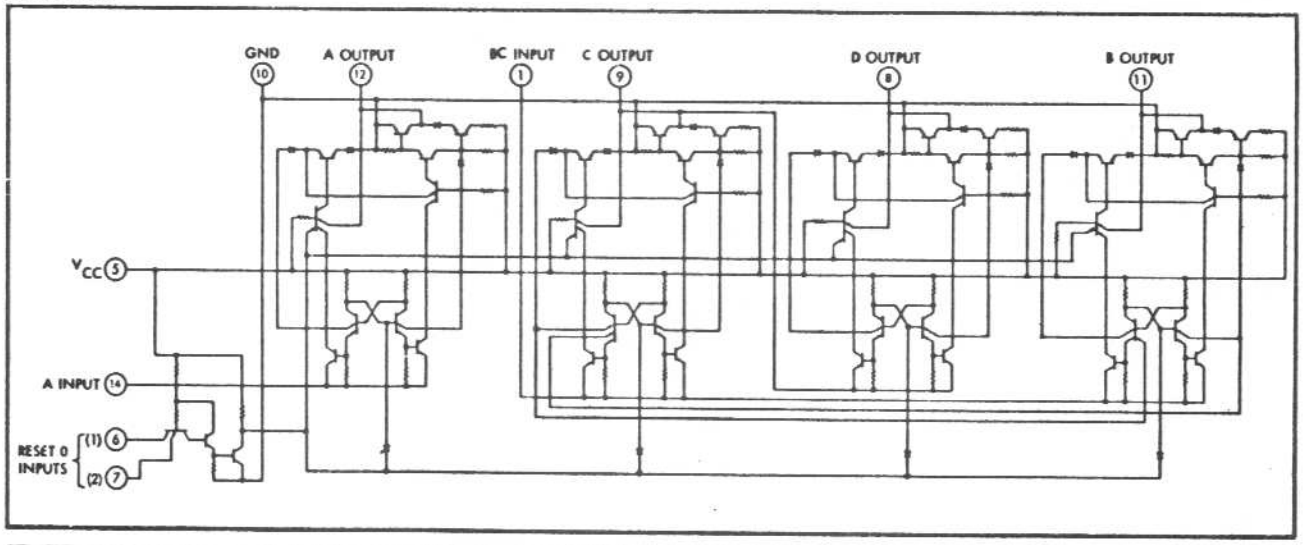
description

The SN7492N is a high-speed monolithic 4-bit binary counter consisting of four master slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-six counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a divide-by-twelve counter, output A must be externally connected to input BC. The input count pulses are applied to input A. Simultaneous divisions of 2, 6, and 12 are performed at the A, C, and D outputs as shown in the truth table above.
2. When used as a divide-by-six counter, the input count pulses are applied to input BC. Simultaneously frequency divisions of 3 and 6 are available at the C and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the divide-by-six counter.

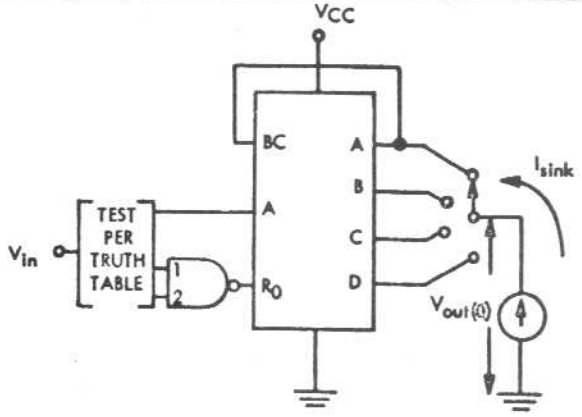
The SN7492N is completely compatible with Series 74 and 74 930 TTL, and Series 15 830 DTL logic families. Average power dissipation is 155 mW.

schematic



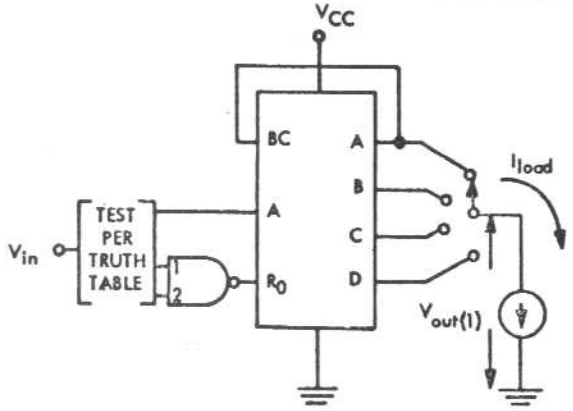
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



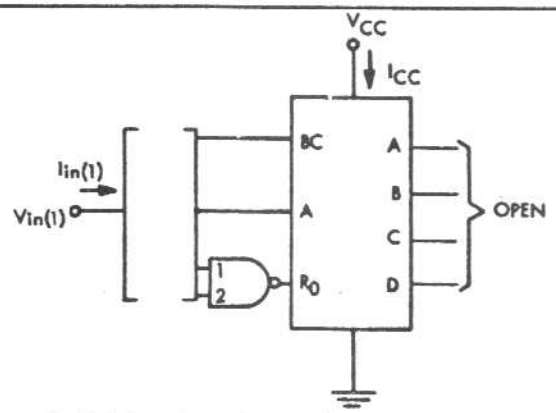
1. Each output is tested in the logical 0 state.

FIGURE 1



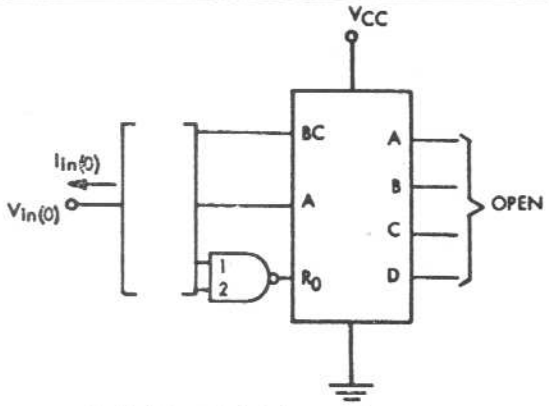
1. Each output is tested in the logical 1 state.

FIGURE 2



1. Each input is tested separately.
2. When testing $R_0(1)$ ground $R_0(2)$.
3. When testing $R_0(2)$ ground $R_0(1)$.
4. When testing I_{CC} reset all outputs to logical 0, ground all inputs, then measure I_{CC}.

FIGURE 3

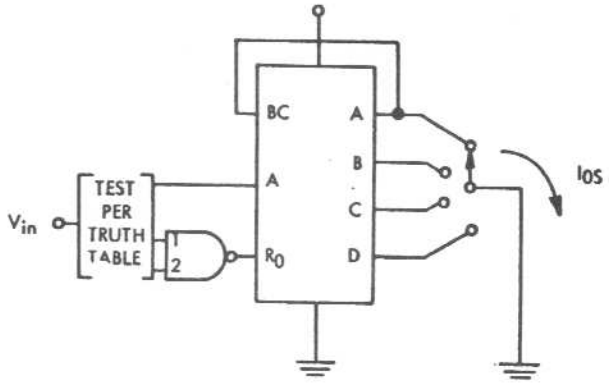


1. Each input is tested separately.
2. When testing $R_0(1)$ apply 4.5 V to $R_0(2)$.
3. When testing $R_0(2)$ apply 4.5 V to $R_0(1)$.

FIGURE 4

†Arrows indicate actual direction of current flow.

d-c test circuits† (continued)

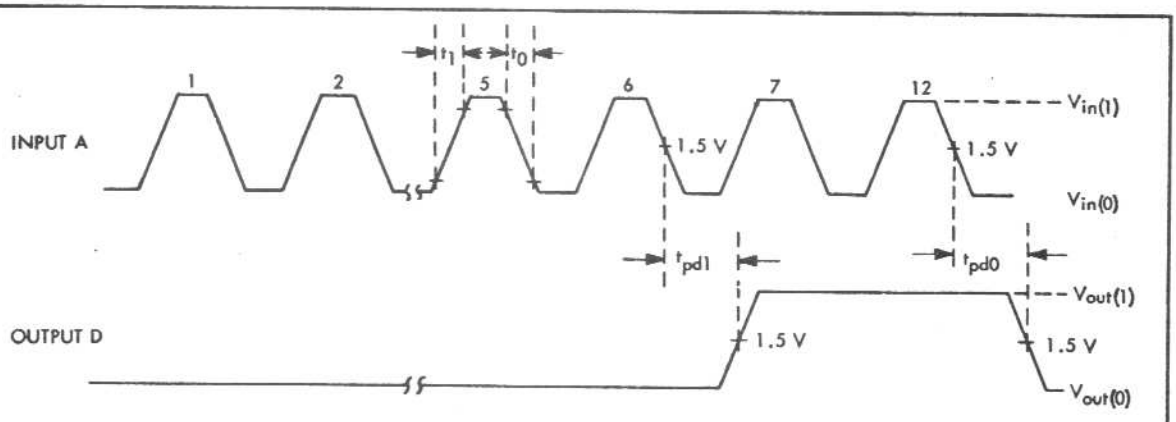


1. Each output is tested in the logical 1 state.

FIGURE 5

†arrows indicate actual direction of current flow

switching time voltage waveforms



1. Input pulse characteristics: $V_{in(1)} \geq 2.4$ V, $V_{in(0)} = 0.4$ V, $t_1 = t_0 \leq 10$ ns, PRR = 1 MHz, duty cycle = 50%.

FIGURE 6 - SWITCHING TIME VOLTAGE WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V

Input Voltage V_{in} (See Notes 3 and 4) . . . . . 5.5 V

Operating Free-Air Temperature Range . . . . . 0°C to 70°C

Storage Temperature Range . . . . . −55°C to 125°C

NOTES: 3. These voltage values are with respect to network ground terminal

4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V

Fan-Out From Each Output (See Note 5) . . . . . 1 to 10

Width of Input Count Pulse, $t_{p(in)}$ . . . . . ≥ 50 ns

Width of Reset Pulse, $t_{p(reset)}$ . . . . . ≥ 50 ns

NOTES: 5. Fan-out from output A to input BC and to 10 additional Series 74 loads is permitted.

electrical characteristics, T_A = 0°C to 70°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at inputs A, $R_{0(1)}$, and $R_{0(2)}$	1	V_{CC} = 4.75 V	2			V
$V_{in(1)}$	Input voltage required to ensure logical 1 at input BC	1	V_{CC} = 4.75 V	2.2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at inputs A, $R_{0(1)}$, and $R_{0(2)}$	2	V_{CC} = 4.75 V			0.8	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at input BC	2	V_{CC} = 4.75 V			0.6	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 V, I_{load} = −400 µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 V, I_{sink} = 16 mA			0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	µA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at input A	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			80	µA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at input BC	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			160	µA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	4	V_{CC} = 5.25 V, V_{in} = 0.4 V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A	4	V_{CC} = 5.25 V, V_{in} = 0.4 V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BC	4	V_{CC} = 5.25 V, V_{in} = 0.4 V			-6.4	mA
I_{OS}	Short-circuit output current †	5	V_{CC} = 5.25 V, V_{out} = 0	-18		-57	mA
I_{CC}	Supply Current	3	V_{CC} = 5 V, T_A = 25°C		31		mA

†Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses			10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	6			60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count Pulse to output D	6			60	100	ns

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
4-Bit Binary Counter

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheets 4,5 & 6

4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7493N
Sprague Part No. USN7493A
National Semiconductor Corp. Part No. DM8533N

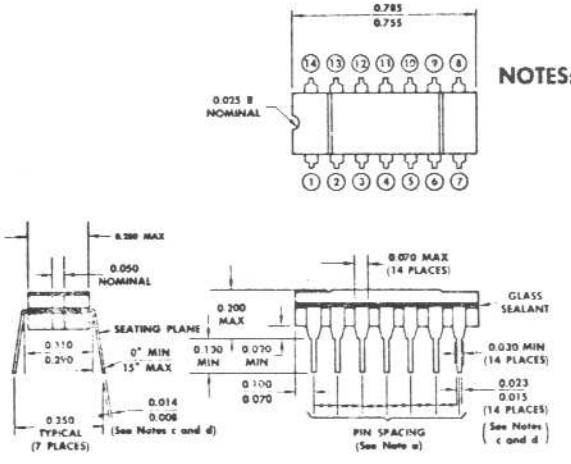
NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.	FOXBORO	THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
REMOVE BURRS & SHARP EDGES	DRAFTSMAN R. Walker 1/24/72		
DIMENSIONS ARE IN INCHES	DESIGNER	TITLE:	CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN74 93N
TOLERANCES ON FRACTIONS: ± 1/64 DECIMALS: ± .005 ANGLES: ± 1/2°	CHECKER R. Walker 1/24/72		
MATERIAL: N/A	ENGINEER [illegible]	SIZE A	SYMBOL B
FINISH: N/A	RELEASED		DRAWING NO. V3008FN
	LOCAL RELEASE	SCALE: NONE	SHEET 1 OF 6

REV A

FORM 6055A (6/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

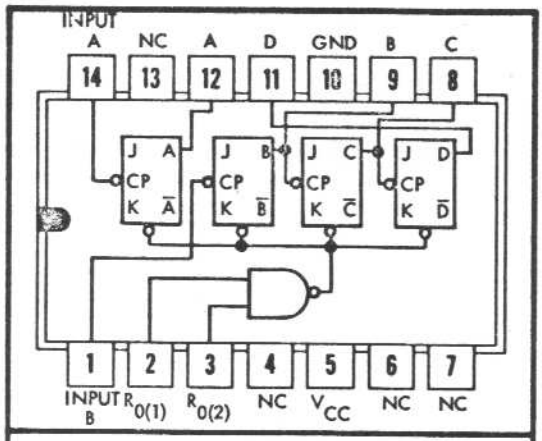
14-PIN FUNCTIONS

THE FOXBORO COMPANY SYSTEMS DIVISION	B | V3008 FN	Rev. A
	Sheet 2 of 5	

logic

TRUTH TABLE (See Notes 1 and 2)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1



positive logic

See truth table

NOTES: 1. Output A connected to input B.
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.

description

The SN7493N is a high-speed, monolithic 4-bit binary counter consisting of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

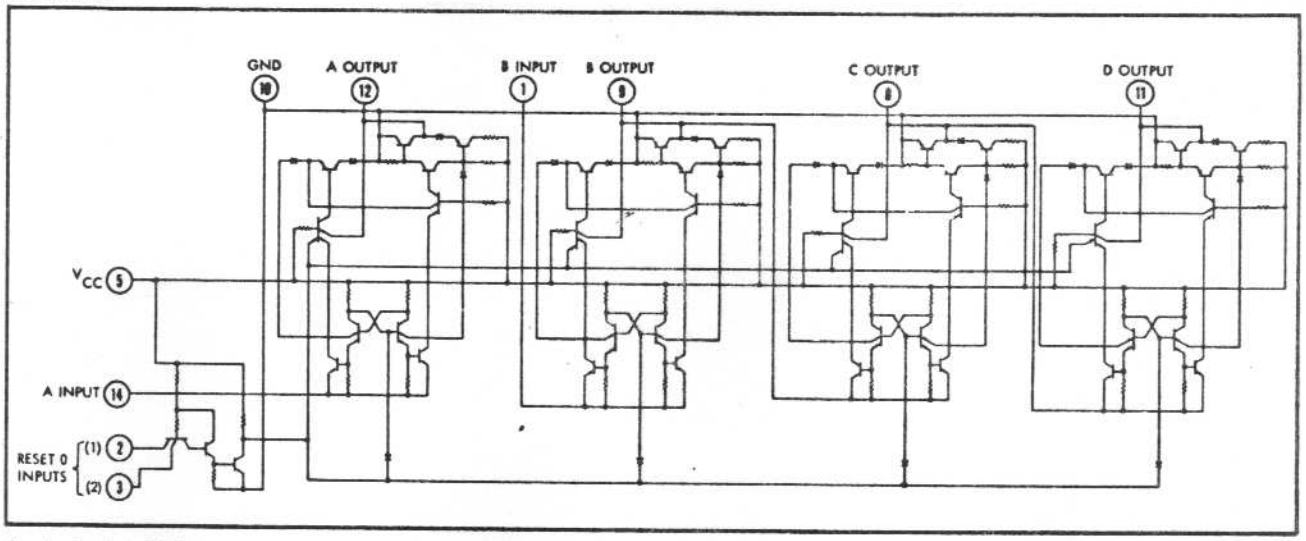
1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

The SN7493N is completely compatible with Series 74 and Series 74 930 TTL, and Series 15 830 DTL logic families. Average power dissipation is 32 mW per flip-flop (128 mW total).

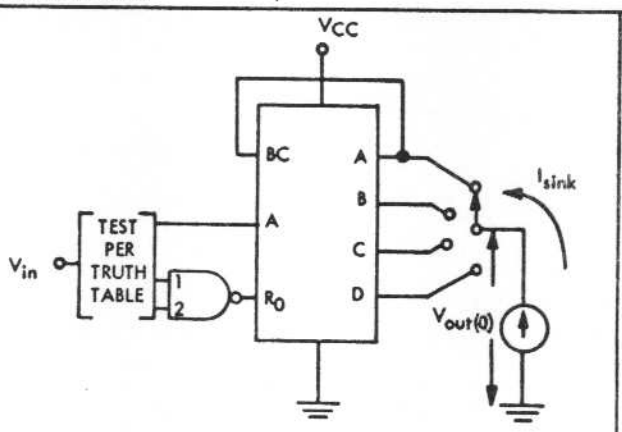
IDENTICAL TO SC 9497

PARAMETER MEASUREMENT INFORMATION

schematic

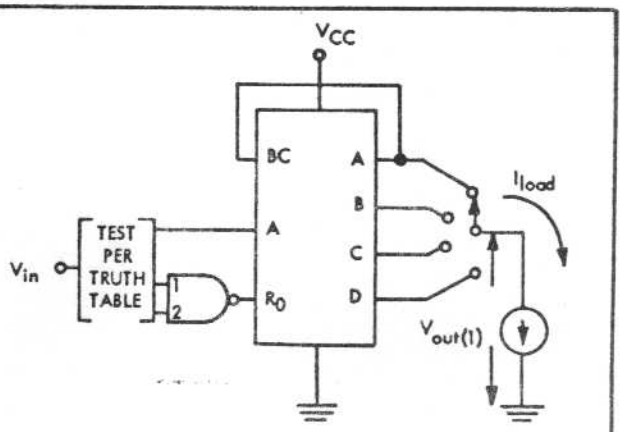


d-c test circuitst



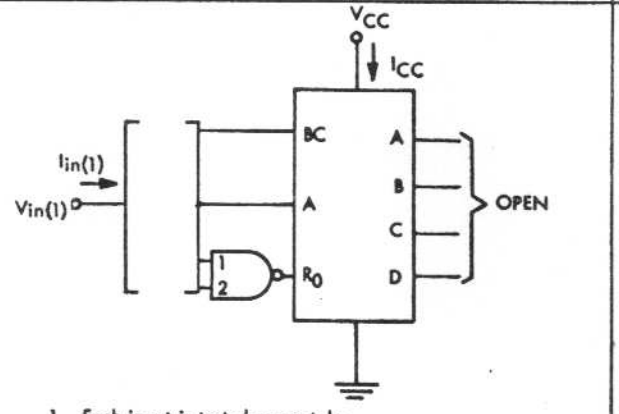
1. Each output is tested in the logical 0 state.

FIGURE 1



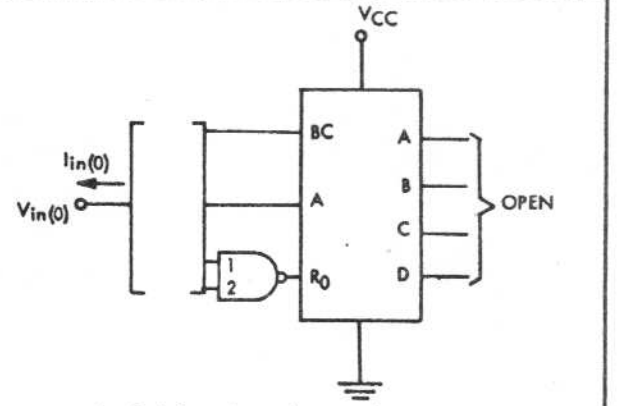
1. Each output is tested in the logical 1 state.

FIGURE 2



1. Each input is tested separately.
2. When testing $R_0(1)$ ground $R_0(2)$.
3. When testing $R_0(2)$ ground $R_0(1)$.
4. When testing I_{CC} all inputs and outputs are open.

FIGURE 3



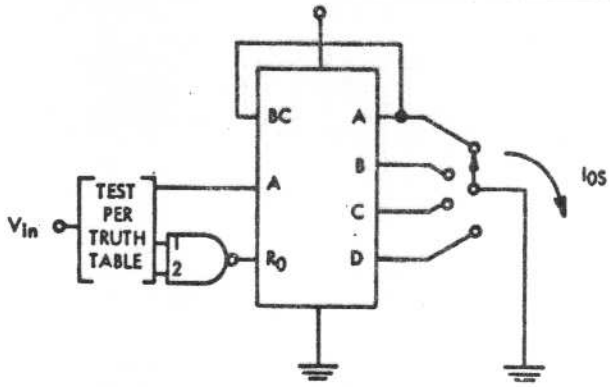
1. Each input is tested separately.
2. When testing $R_0(1)$ apply 4.5 V to $R_0(2)$.
3. When testing $R_0(2)$ apply 4.5 V to $R_0(1)$.

FIGURE 4

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

d-c test circuitst (continued)

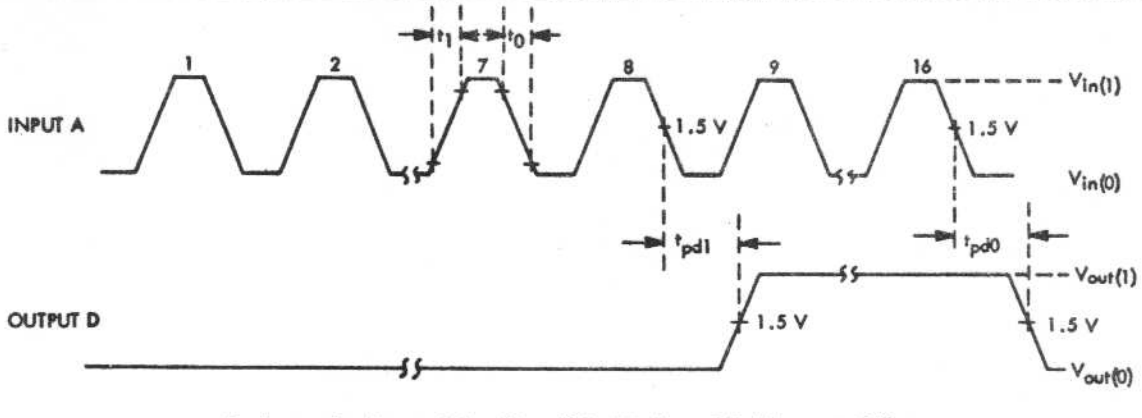


1. Each output is tested in the logical 1 state.

FIGURE 5

tarrows indicate actual direction of current flow

switching time voltage waveforms



1. Input pulse characteristics: $V_{in(1)} \geq 2.4$ V, $V_{in(0)} \leq 0.4$ V, $t_1 = t_0 \leq 10$ ns, PRR = 1 MHz, duty cycle = 50%.

FIGURE 6 - SWITCHING TIME VOLTAGE WAVEFORMS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V
Input Voltage V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Free-Air Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . . . -55°C to 125°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

Supply Voltage V_{CC} . . . . . 4.75 V to 5.25 V
Fan-Out From Each Output (See Note 5) . . . . . 1 to 10
Width of Input Count Pulse, $t_{p(in)}$ . . . . . ≥ 50 ns
Width of Reset Pulse, $t_{p(reset)}$ . . . . . ≥ 50 ns

NOTES: 5. Fan-out from output A to input B and to 10 additional Series 74 loads is permitted.

electrical characteristics, T_A = 0°C to 70°C

PARAMETER		TEST FIG.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at inputs A, $R_{0(1)}$, and $R_{0(2)}$	1	V_{CC} = 4.75 V	2			V
$V_{in(1)}$	Input voltage required to ensure logical 1 at input B	1	V_{CC} = 4.75 V	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at inputs A, $R_{0(1)}$, and $R_{0(2)}$	2	V_{CC} = 4.75 V			0.8	V
$V_{in(0)}$	Input voltage required to ensure logical 0 at input B	2	V_{CC} = 4.75 V			0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 V, I_{load} = -400 µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 V, I_{sink} = 16 mA			0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			40	µA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	3	V_{CC} = 5.25 V, V_{in} = 2.4 V			80	µA
			V_{CC} = 5.25 V, V_{in} = 5.5 V			1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	4	V_{CC} = 5.25 V, V_{in} = 0.4 V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	4	V_{CC} = 5.25 V, V_{in} = 0.4 V			-3.2	mA
I_{os}	Short-circuit output current †	5	V_{CC} = 5.25 V, V_{out} = 0	-18		-57	mA
I_{CC}	Supply current	3	V_{CC} = 5 V		32		mA

† Not more than one output should be shorted at a time

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIG.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses			10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	6			75	135	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	6			75	135	ns

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
4-Bit Shift Register

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 5

4. MANUFACTURER'S NAME AND PART NO.

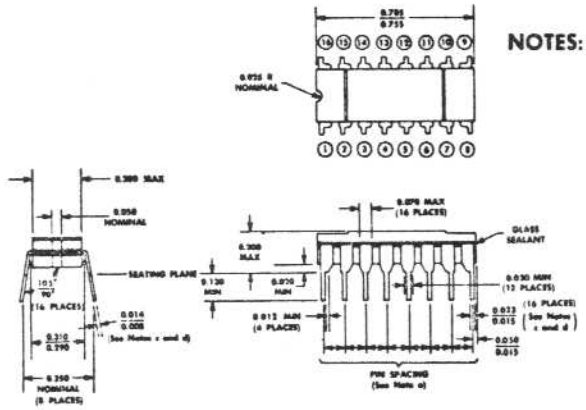
Texas Instrument, Part No. SN7494N

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED	WORK AUTH NO.		THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
REMOVE BURRS & SHARP EDGES DIMENSIONS ARE IN INCHES ALL DIMS APPLY AFTER PLATING	DRAFTSMAN R. Walden 1/24/	DATE	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN7494N
DECIMAL PLACES ON FRACTIONS: ± 1/64 DECIMALS: ± .005 ANGLES: ± 1/2°	DESIGNER		
	CHECKER R. Walden 3/24/		
MATERIAL: N/A	ENGR.	3/	SIZE A | SYMBOL | DRAWING NO. V3008FP | REV A
FINISH: N/A	RELEASED		
	LOCAL RELEASE		SCALE: NONE | SHEET 1 OF 5

FORM 5083A (6/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (1) and (16)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

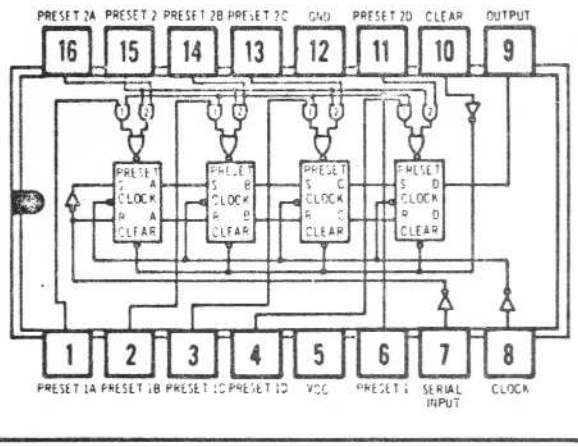
16-PIN FUNCTIONS

description

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs 1A through 1D are activated during the time that a positive pulse is applied to present 1 if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active.



positive logic

High input to clear sets A, B, C and D to logical 0.

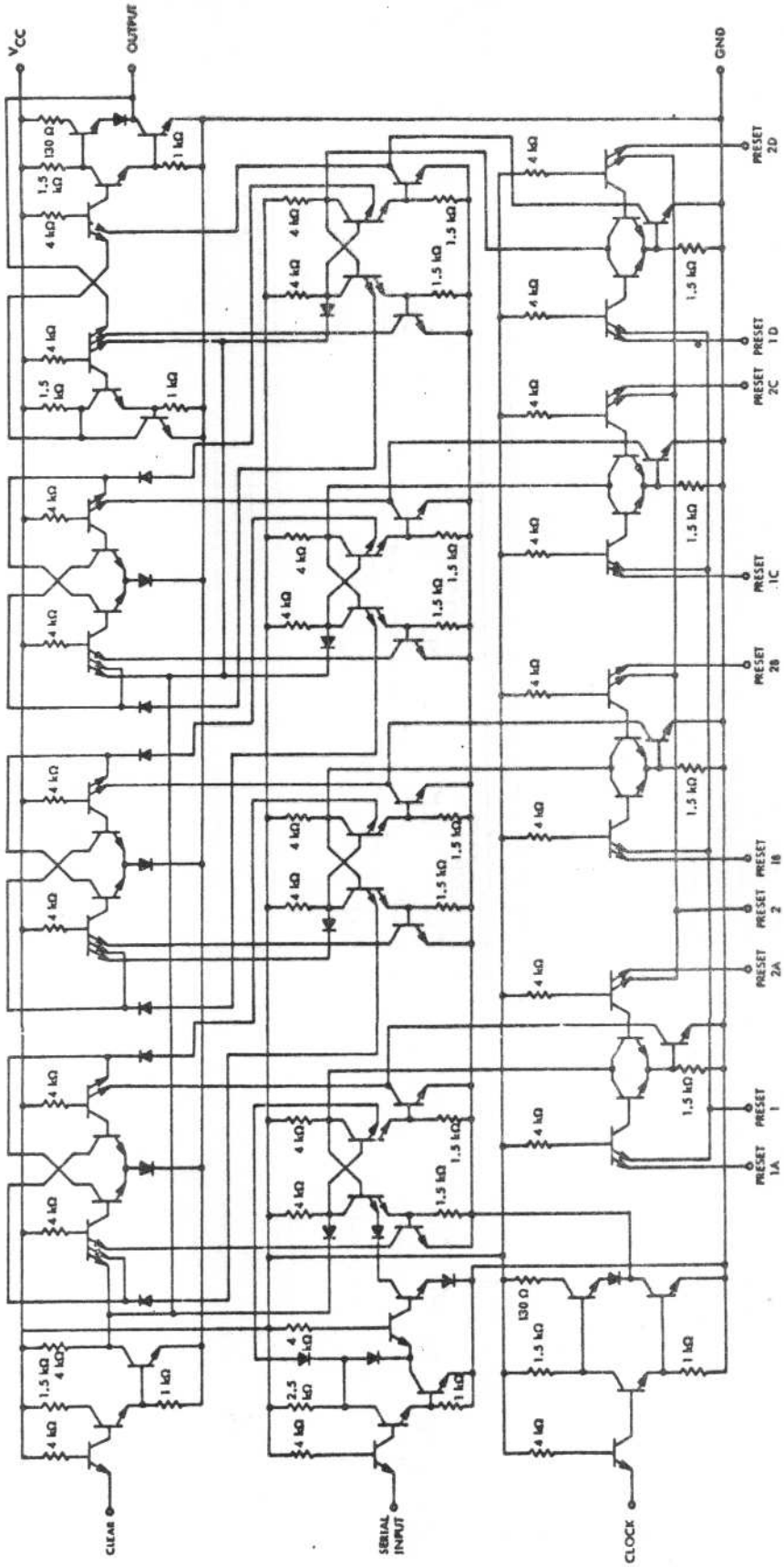
Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input and either preset 1 or preset 2 must be at a logical 0 when clocking occurs.

This register is completely compatible for use with TTL and DTL logic circuits and when used with other TTL circuits typical one volt noise margins are maintained. Typical average power dissipation is 175 milliwatts, and propagation delay times from clock to output are typically 40 nanoseconds.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	-55°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.



Component values shown are nominal.

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	Sheet 4 of 5	

Form 5039 (6/68)

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1)	4.75	5	5.25	V
Fan-Out from Output			10	
Width of Clock Pulse, $t_{p(clock)}$	35			ns
Width of Clear Pulse, $t_{p(clear)}$	30			ns
Width of Preset Pulse, $t_{p(preset)}$	30			ns
Serial Input Setup Time: $t_{setup(1)}$	35			ns
$t_{setup(0)}$	25			ns
Serial Input Hold Time, t_{hold}	0			

NOTE 1: These voltage values are with respect to network ground terminal.

electrical characteristics (over operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400 μA	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16 mA		0.22‡	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except Preset 1 and Preset 2	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
		V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at Preset 1 and Preset 2	V_{CC} = MAX, V_{in} = 2.4 V			160	μA
		V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(0)}$	Logical 0 level input current at any input except Preset 1 and Preset 2	V_{CC} = MAX, V_{in} = 0.4 V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at Preset 1 and Preset 2	V_{CC} = MAX, V_{in} = 0.4 V			-6.4	mA
I_{OS}	Short-circuit output current¶	V_{CC} = MAX, V_{out} = 0	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX		35‡	57	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ These typical values are at V_{CC} = 5 V, T_A = 25°C.
¶ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from Preset to output	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15 pF, R_L = 400 Ω			40	ns

FIRST USED ON	REVISIONS				
	LTR	DESCRIPTION	DR	DATE	APPROVED
	A	LOCAL RELEASE ECN NO. 1912			

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
4-Bit Shift Register Right Shift - Left Shift

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 2

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheets 5,6,7,8 & 9

4. MANUFACTURER'S NAME AND PART NO.

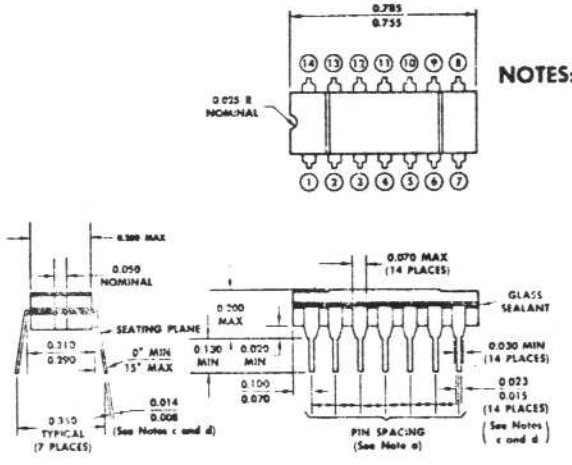
Texas Instrument, Part No. SN7495N

NOTE: Only the item described on this drawing when procured from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

DO NOT SCALE PRINT

UNLESS OTHERWISE SPECIFIED ALL EDGES SHARP & BURR FREE DIMENSIONS ARE IN INCHES FINISHES APPLY AFTER PLATING TOLERANCES ON FRACTIONS: ± 1/64 DECIMALS: ± .005 ANGLES: ± 1/2° MATERIAL: N/A FINISH: N/A	WORK AUTH NO.		THE FOXBORO COMPANY FOXBORO, MASSACHUSETTS, U.S.A.
	DRAFTSMAN B. Weller	DATE 3/29/68	TITLE: CIRCUIT, INTEGRATED DUAL IN-LINE PACKAGE TYPE SN74 95N
	DESIGNER		
	CHECKED B. Weller	3/29/68	
	ENGINEER	3/[illegible]	SIZE A | SYMBOL | DRAWING NO. V3008FR | REV A
	RELEASED		
	LOCAL RELEASE		SCALE: NONE | SHEET 1 OF 9

FORM 5003A (6/67)



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (4) and (11)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

e. All JEDEC TO-116 notes apply.

14-PIN FUNCTIONS

description

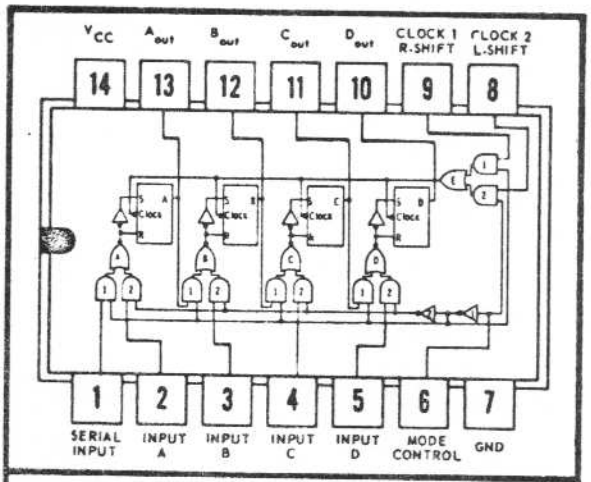
This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR gate, and six inverter-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

When a logical 0 level is applied to the mode control input, the number 1 AND gates are enabled and the number 2 AND gates are inhibited. In this mode the output of each flip-flip is coupled to the R-S inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number 2 AND gates.

When a logical 1 level is applied to the mode control input, the number 1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number 2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register or, with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (D_{out} to input C, and etc.), and serial data is entered at input D.

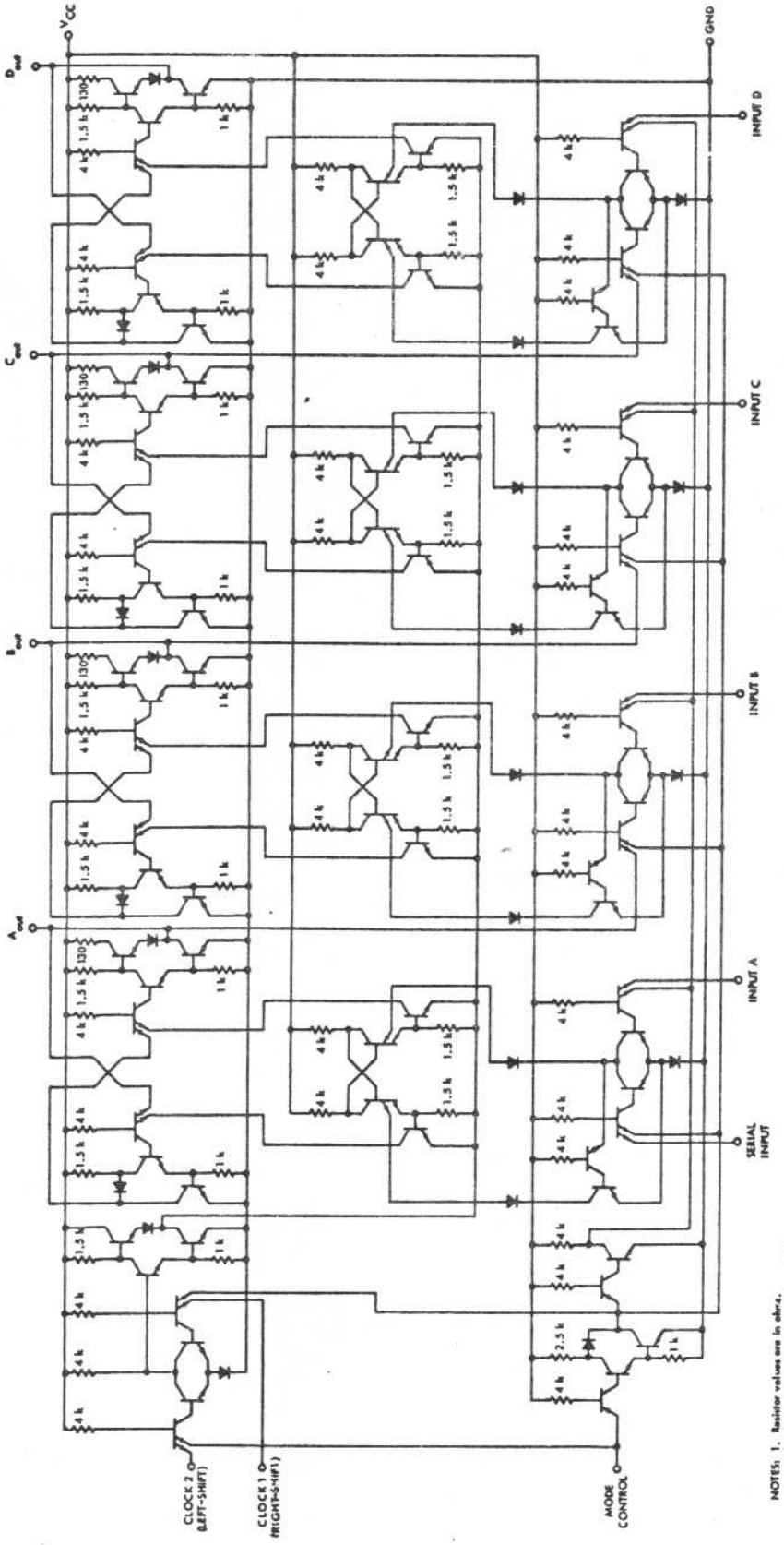
Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking.

The shift register is completely compatible with Series 74 and Series 15 830 DTL logic families. Average power dissipation is typically 250 milliwatts.



positive logic

Mode control = 0 for right shift
Mode control = 1 for left shift or parallel load



THE FOXBORO COMPANY SYSTEMS DIVISION	V3008FR	Rev. A
	Sheet 4 of 5	

d-c test circuits†

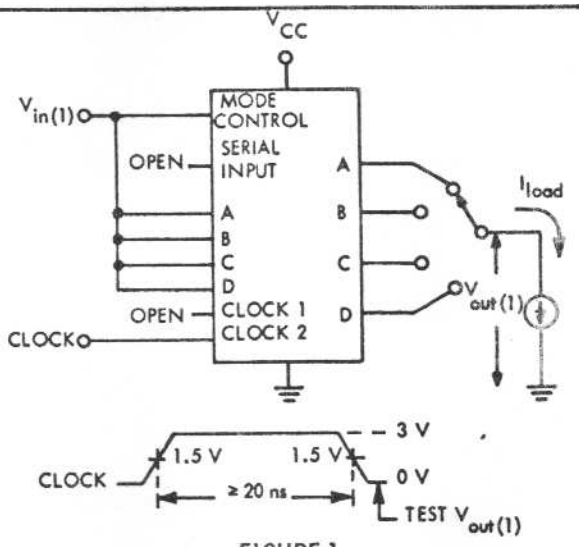


FIGURE 1

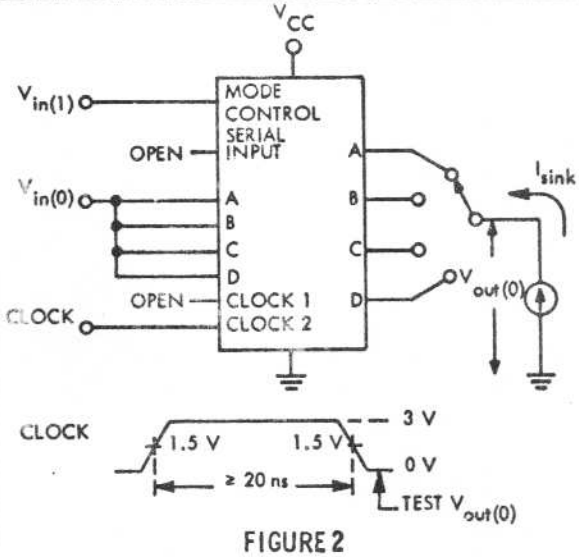


FIGURE 2

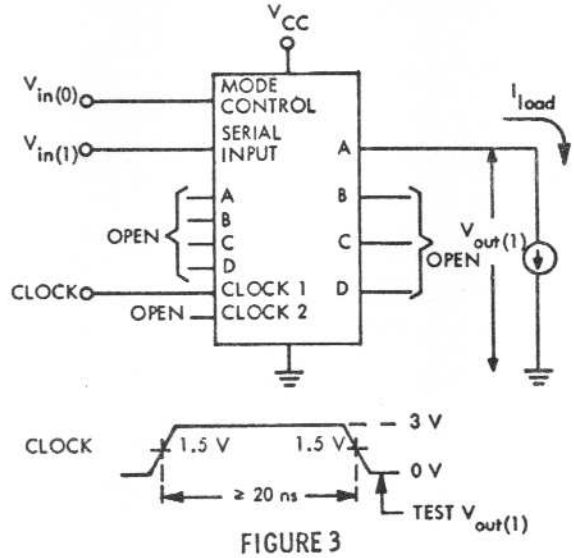


FIGURE 3

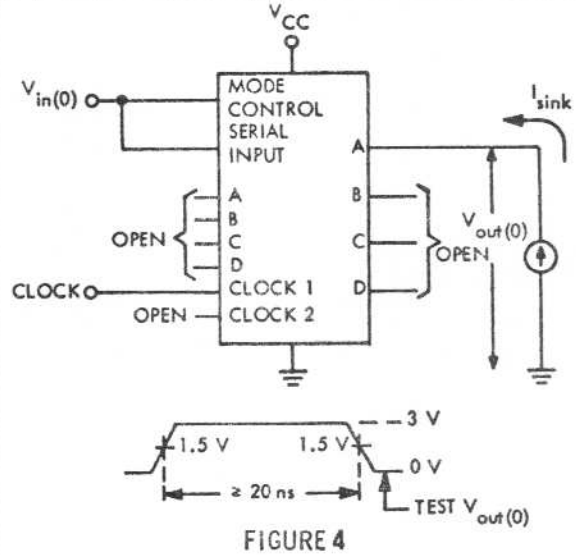
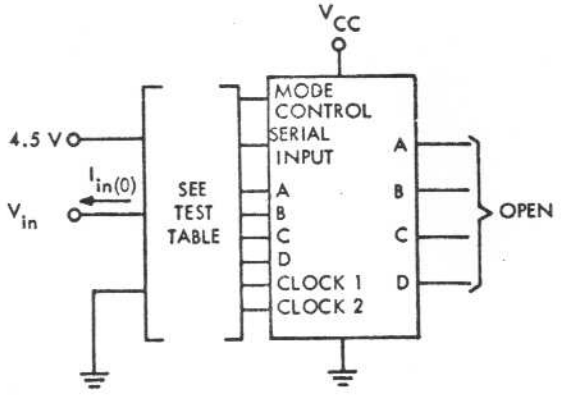


FIGURE 4



1. Each input is tested separately.

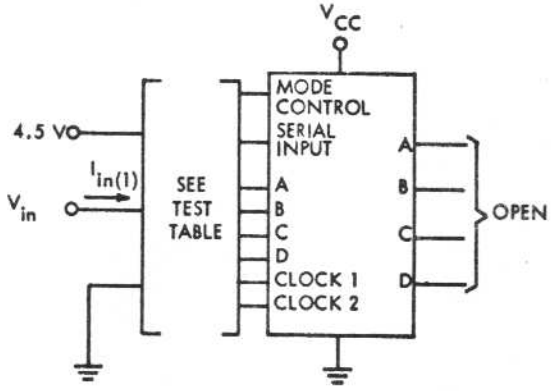
TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INPUT	NONE	MODE CONTROL
INPUT A	MODE CONTROL	NONE
INPUT B	MODE CONTROL	NONE
INPUT C	MODE CONTROL	NONE
INPUT D	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

FIGURE 5

†Arrows indicate actual direction of current flow.

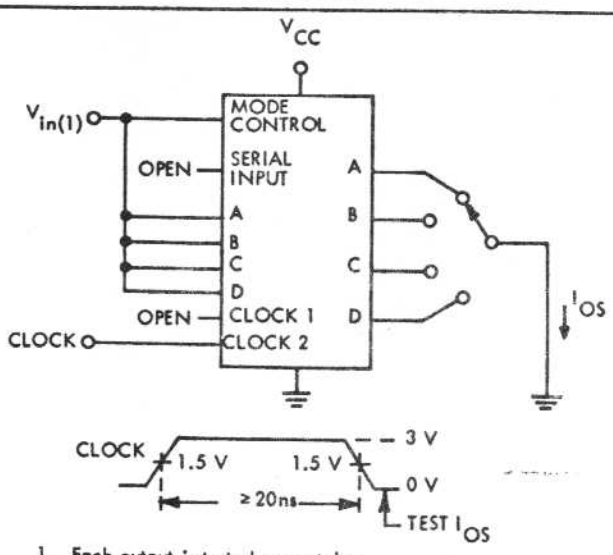
d-c test circuits † (continued)



TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	NONE	CLOCK 2
SERIAL INPUT	MODE CONTROL	NONE
INPUT A	NONE	MODE CONTROL
INPUT B	NONE	MODE CONTROL
INPUT C	NONE	MODE CONTROL
INPUT D	NONE	MODE CONTROL
CLOCK 1	MODE CONTROL	NONE
CLOCK 2	NONE	MODE CONTROL

FIGURE 6



1. Each output is tested separately.

FIGURE 7

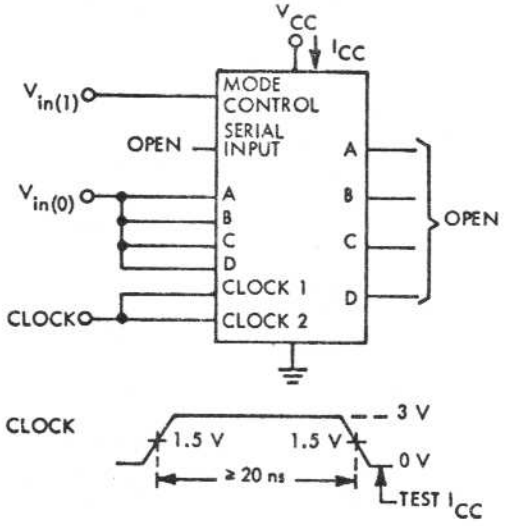
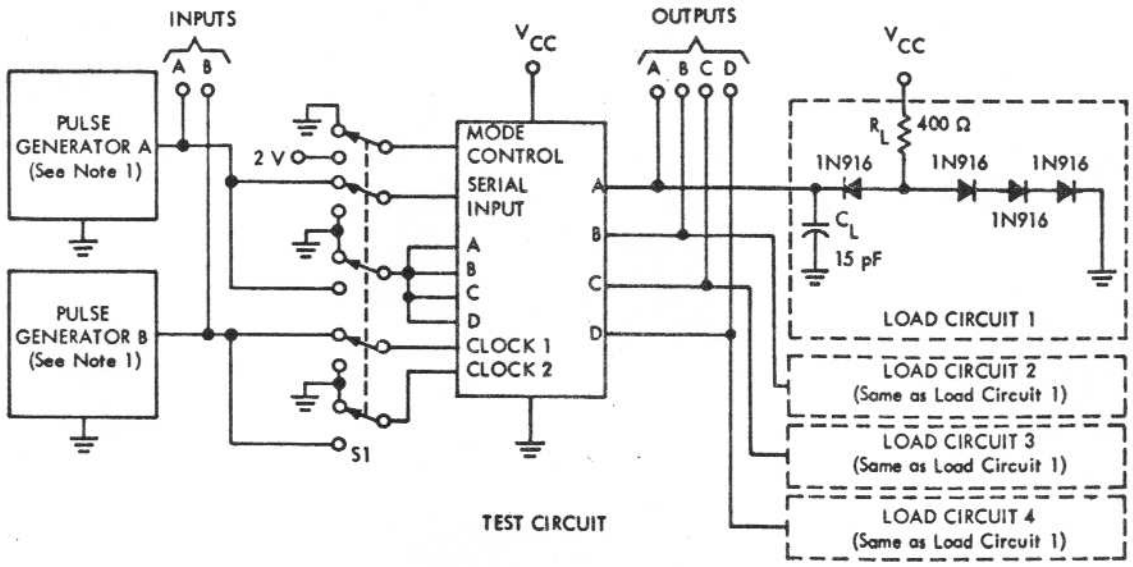


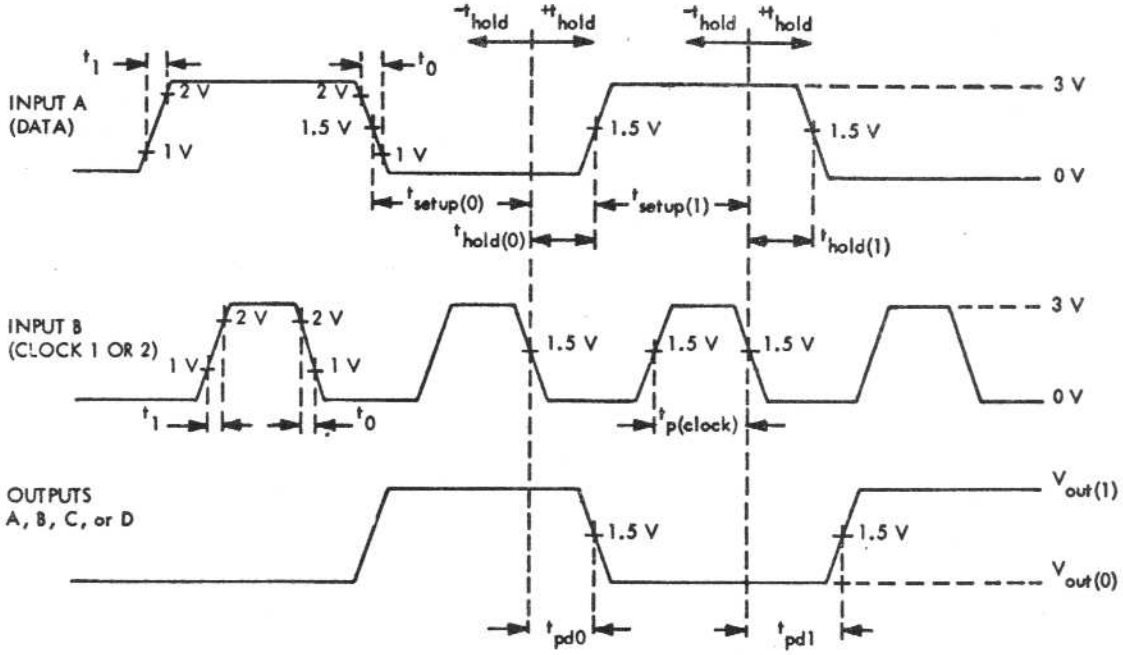
FIGURE 8

†Arrows indicate actual direction of current flow.

switching characteristics



TEST CIRCUIT



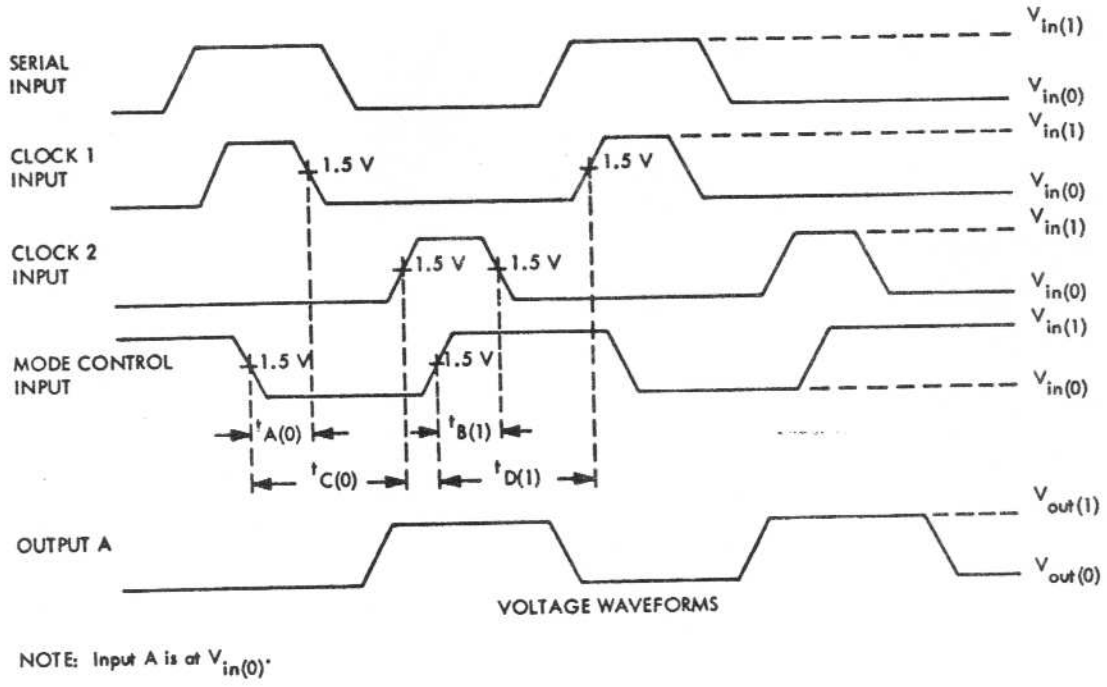
VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, t_1 = 12 to 16 ns, t_0 = 3 to 5 ns, and $Z_{out} \approx 50\ \Omega$. For pulse generator A : $t_p \geq 20$ ns and PRR = 500 kHz. For pulse generator B : $t_p \geq 15$ ns and PRR = 1 MHz. When testing f_{max} vary PRR.

2. Voltage values are with respect to network ground terminal.
3. C_L includes probe and jig capacitance.

FIGURE 9 — SWITCHING TIMES

recommended mode control setup times



NOTE: Input A is at $V_{in(0)}$.

FIGURE 10 — MODE CONTROL SETUP TIMES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −55°C to 150°C

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1)	4.75	5	5.25	V
Fan-Out From Each Output			10	
Width of Clock Pulse $t_{p(clock)}$ (See Figure 9)	15	10		ns
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup} (See Figure 9)	20	10		ns
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold} (See Figure 9)	0	−10		ns
Logical 0 Level Setup Time Required at Mode Control $t_{A(0)}$ (See Figure 10) (With Respect to Clock 1 input)	20			ns
Logical 1 Level Setup Time Required at Mode Control $t_{B(1)}$ (See Figure 10) (With Respect to Clock 2 input)	15			ns
Logical 0 Level Setup Time Required at Mode Control $t_{C(0)}$ (See Figure 10) (With Respect to Clock 2 input)	10			ns
Logical 1 Level Setup Time Required at Mode Control $t_{D(1)}$ (See Figure 10) (With Respect to Clock 1 input)	10			ns

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_{In(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 3	V_{CC} = MIN	2			V
$V_{In(0)}$	Input voltage required to ensure logical 0 at any input terminal	2 and 4	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 and 3	V_{CC} = MIN, I_{load} = −400 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2 and 4	V_{CC} = MIN, I_{sink} = 16 mA			0.4	V
$I_{In(0)}$	Logical 0 level input current at any input except mode control	5	V_{CC} = MAX, V_{In} = 0.4 V			−1.6	mA
$I_{In(0)}$	Logical 0 level input current at mode control	5	V_{CC} = MAX, V_{In} = 0.4 V			−3.2	mA
$I_{In(1)}$	Logical 1 level input current at any input except mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{In} = 5.5 V			1	mA
$I_{In(1)}$	Logical 1 level input current at mode control	6	V_{CC} = MAX, V_{In} = 2.4 V			80	μA
			V_{CC} = MAX, V_{In} = 5.5 V			1	mA
I_{OS}	Short-circuit output current ‡	7	V_{CC} = MAX	−18		−57	mA
I_{CC}	Supply current	8	V_{CC} = MAX		50†	85	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡ Not more than one output should be shorted at a time.
† This typical value is at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	9	C_L = 15 pF, R_L = 400 Ω	20	31		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF, R_L = 400 Ω		26	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF, R_L = 400 Ω		24	35	ns

REVISIONS

LTR	DESCRIPTION	CODE	DATE	REVISED BY APPROVED BY
A	LOCAL RELEASE PER ECN 1912.			

REV STATUS OF SHEETS	REV	A	A	A	A	A	A										
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

TOLERANCES UNLESS OTHERWISE SPECIFIED
DECIMAL DIMENSIONS ± .020
ANGLES ± 1°

	DRAWN	CHK'D	DATE
	B. WALKER	B. WALKER	2/21/69
DRAFTING			
DESIGNED			
APPROVED	J. P. DENGLER		
LOCAL RELEASE	M. J. COOK		7/11/69
CORPORATE RELEASE	M. FOWLER		

FOXBORO

THE FOXBORO COMPANY
FOXBORO, MASSACHUSETTS, U.S.A.

TITLE
CIRCUIT, INTEGRATED
DUAL IN-LINE PACKAGE
TYPE SN7496N

SUPERSEDING
INTERCHANGEABLE YES NO
SIMILAR TO

DESIGNED FOR

SIZE A B

DRAWING NUMBER
V3008FS

SCALE

WT

SHEET 1 OF 6

FORM 5758-C (5/69)

1. DESCRIPTION

Circuit, Integrated (Dual In-Line Package)
5-Bit Shift Register

2. PHYSICAL CHARACTERISTICS

2.1 See Sheet 3.

3. PERFORMANCE CHARACTERISTICS

3.1 See Sheet 6.

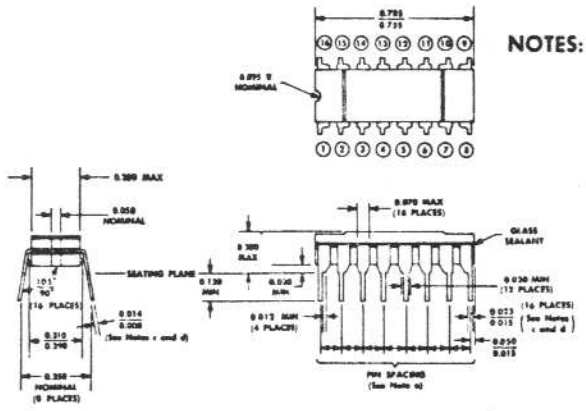
4. MANUFACTURER'S NAME AND PART NO.

Texas Instrument, Part No. SN7496N

NOTE: Only the item described on this drawing when procurred from the manufacturers listed hereon for use. A substitute item shall not be used without Engineering approval.

SIZE	SYMBOL	DRAWING NO.	REV
A	B	V3008FS	A
SCALE:		SHEET 2 OF	

DO NOT SCALE PRINT



NOTES:

a. The true-position pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its true longitudinal position relative to pins (1) and (16)

b. All dimensions in inches unless otherwise noted.

c. This dimension does not apply for solder-dipped leads.

d. When solder-dipped leads are specified dipped area of the lead extends from the lead tip to at least 0.020 inch above the seating plane.

16-PIN FUNCTIONS

THE FOXBORO COMPANY SYSTEMS DIVISION	B	V3008 FS	Rev. A
		Sheet 3 of	

Form 5039 (6/68)

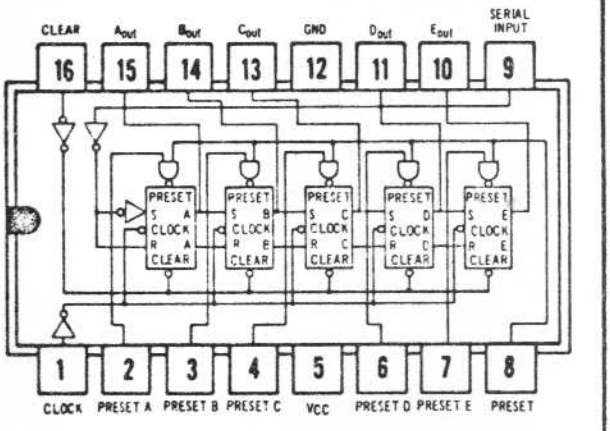
description

The SN7496N consists of five R-S master-slave flip-flops connected as a shift register to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The common preset input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input.

Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.



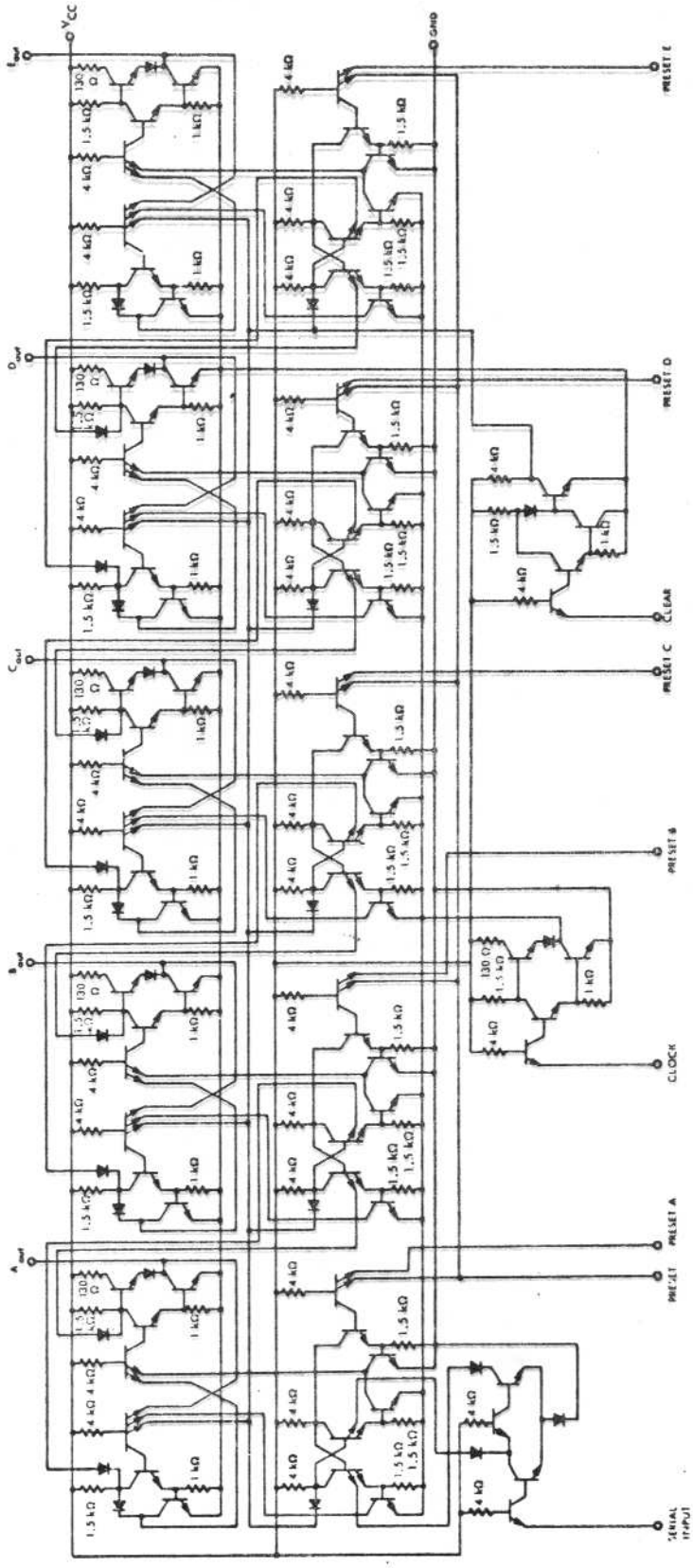
positive logic

Low input to clear sets all outputs to logical 0.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	-55°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.



THE FOXBORO COMPANY SYSTEMS DIVISION	B V3008FS	Rev. A
	Sheet 5 of	

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1)	4.75	5	5.25	V
Fan-Out from Output			10	
Width of Clock Pulse, $t_{p(clock)}$	35			ns
Width of Clear Pulse, $t_{p(clear)}$	30			ns
Width of Preset Pulse, $t_{p(preset)}$	30			ns
Serial Input Setup Time, t_{setup}	30			ns
Serial Input Hold Time, t_{hold}	0			ns

NOTE 1: This voltage value is with respect to network ground terminal.

electrical characteristics (over operating free-air temperature range unless otherwise noted)

	PARAMETER	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = -400 μA	2.4	3.5‡		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16 mA		0.22‡	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except Preset (pin ⑧)	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
		V_{CC} = MAX, V_{in} = 5.5 V			-1	mA
$I_{in(1)}$	Logical 1 level input current at Preset (pin ⑧)	V_{CC} = MAX, V_{in} = 2.4 V			200	μA
		V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(0)}$	Logical 0 level input current at any input except Preset (pin ⑧)	V_{CC} = MAX, V_{in} = 0.4 V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at Preset (pin ⑧)	V_{CC} = MAX, V_{in} = 0.4 V			-8	mA
I_{OS}	Short-circuit output current ¶	V_{CC} = MAX, V_{out} = 0	-18		-57	mA
I_{CC}	Supply current	V_{CC} = MAX		48‡	79	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ Those typical values are at V_{CC} = 5 V and T_A = 25°C.
¶ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from preset to output	C_L = 15 pF, R_L = 400 Ω			40	ns